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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

JOSEPH T. EVANS, JR., ET AL.

Serial No.: 582,672
Filed: September 14, 1990
Group: 233
Examiner: Alyssa H. Bowler
For: NON-VOLATILE MEMORY CIRCUIT USING FERROELECTRIC CAPACITOR STORAGE ELEMENT

RECEIVED
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GROUP 230

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

DECLARATION OF LEO N. CHAPIN

I, Leo N. Chapin, of 1503 Yukon Drive, Sunnyvale, California 94087, do hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, do hereby declare as follows:

1. I was employed at Krysalis Corporation, Albuquerque, New Mexico, from December 4, 1985, to September 1, 1989, when the assets thereof were purchased by National Semiconductor Corporation of Santa Clara, California.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
Commissioner of Patents and Trademarks,
Washington, D.C. 20231 on July 8, 1991
(Date of Deposit)
Roger N. Chauza, Reg. No. 29,753
Name of Applicant, assignee, or Registered Representative
Signature
July 8, 1991
Date of Signature

2. My job title during the years of 1986 and 1987 was Research Associate and my responsibilities were the synthesis of sol-gels and the depositions of all ferroelectric films on substrates.

To the best of my knowledge, the integration of ferroelectric material on silicon to form microelectronic memory circuits was not attempted before, and thus all the processes, techniques and materials had to be developed by Krysalis by experimental and trial and error techniques.

3. Among my various responsibilities while employed at Krysalis, I developed and maintained a log of the wafers that I processed with ferroelectric material.

4. Exhibit A attached hereto is a copy of a "FES Coating Log" that I developed and maintained while employed at Krysalis. The log illustrates various wafers processed at Krysalis between August 2, 1986, and September 29, 1987.

5. The data input into a data base and represented by Exhibit A was carried out by myself while at Krysalis, using a Macintosh personal computer, Model MacPlus, and using a then commercially available program called "Overview". The Overview program is a relational type data base adapted for storing data and presenting the data in desired formats. The FES coating log data was stored on a magnetic three and one-half inch floppy disk during all times, including the present time. I found the computer and software a reliable system for storing and retrieving data for the FES coating log.

6. During the course of gathering evidence for this matter, I recalled that I still had the magnetic disk with the FES coating log data. However, I no longer had the "Overview" program, but instead had a commercially available "Panorama" software data base program used on my Macintosh personal computer. The Panorama program was designed by the original makers of the Overview program, but allows data input by the Overview format to be output under the new program. In printing out the original FES coating log data previously stored on the floppy disk using the Panorama software and the Macintosh personal computer, I inputted column headings for the data to provide the printout of Exhibit A. The actual FES coating log data itself was last changed on the floppy disk November 4, 1987, as indicated at the bottom of each page of the printout of Exhibit A.

7. The "Date Coated" column of Exhibit A indicates the day Krysalis processed wafers by depositing thin film ferroelectric material on the virgin or preprocessed wafers.

8. The "Film ID" column identifies the particular substrate or semiconductor wafer on which the ferroelectric material was deposited by Krysalis.

9. As an example of interpretation of the FES coating log data, on page 9 of the log, semiconductor wafer "6310A" was coated with a ferroelectric material on November 6, 1986.

The other entries in the log associated with the 6310A wafer are identified as follows:

"OrbTD01cmos" under the heading of "Substrate Description" means that the wafer itself was fabricated by Orbit Semiconductor. The wafer was a TD01 test wafer (TW) with CMOS transistor circuits.

"Adeline" was an arbitrary name associated with the "6310A" TD01 wafer as it was processed, tested and evaluated by Krysalis.

Under the column heading "Bel Type", there is noted the different types, if at all, of bottom electrode materials. The question mark for the 6310A CMOS test wafer means that the type of bottom electrode material was unknown to me at the time the data was entered into the log.

After depositing the ferroelectric material, and patterning the material so as to form a capacitor dielectric at various locations on the wafer, the wafer was annealed or sintered at a temperature of 550°C to transform the material into a ferroelectric ceramic that exhibits a hysteresis characteristic.

"G6300" under the column heading "Sol-Gel ID" identifies the date the ferroelectric material was formulated by Krysalis. "G" means a sol-gel type of ferroelectric material. The "6" means 1986, and the "300" means the 300th day of 1986, i.e., October 27, 1986. The term "(8/40/60,+10),10" under the same heading identifies the respective amounts of lanthanum, zirconium and titanium in the PLZT ferroelectric sol-gel material. The "+10" term indicates an atomic percentage of excess lead. The "10" term outside the parenthesis means that a period of ten days passed between the time the ferroelectric sol-gel material itself was formulated and thereafter deposited on the wafer.

The designation "10cts" under the column heading "Coats & Spin, Speed" indicates that ten separate coats or layers of the ferroelectric material were deposited on top of each other to form a composite layer of the ferroelectric dielectric material. The ferroelectric material was spun on the wafer in liquid form at a speed of 2000 rpm.

In the early development efforts at Krysalis, each thin film layer of liquid ferroelectric material was sintered separately for a time period of about forty-five minutes to form a hardened ceramic film. The column heading "Sinter Profile" identifies the sintering temperature. The high temperature sintering effectively converted the film amorphous material into a Perovskite crystalline material that exhibits ferroelectric characteristics. The combined sintering steps themselves often took several hours.

The "Bake Profile" column of the log of Exhibit A has an entry "NA" (not applicable) until about December 17, 1986, at which date the processing of the individual ferroelectric layers was modified. Rather than conducting a high temperature sintering step of each layer, as was previously done, each ferroelectric film layer was baked for a short period of time to drive off organics, and then after the last layer was applied, the entire layered structure was sintered at a higher temperature. For example, the wafer identified with Film ID 6351A on page 10 of the log was processed by baking each layer for two minutes at a temperature of 300°C, i.e., the designation of "2@300" in the "Bake Profile" column of the log. Then, the entire layered ferroelectric material was sintered for thirty minutes at 650°C in an oxygen environment, i.e., the designation of "30@650inO_2" in the "Sinter Profile" column of the log.

10. It is to be noted in the log of Exhibit A that I processed other CMOS wafers bearing Film IDs including 6315B and 6332A through 6342D on dates between November 13, 1986, and December 8, 1986. These CMOS wafers noted in the log were TD01 test wafers, although not identified in the log as such. The TD01 CMOS test wafers each had many die with CMOS transistor memory circuits fabricated by Orbit

Semiconductor, Inc., and with the transistor circuits connected to ferroelectric capacitors as fabricated at Krysalis. Each die of the TD01 CMOS test wafers had a memory cell arrangement with complementary transistors and ferroelectric capacitors.

11. Other CMOS test wafers processed by Krysalis to completion are identified in the log of Exhibit A as follows:

Film ID	Date Coated
7043 B	2/12/87
7044 A	2/13/87
7044 K	2/13/87
7048 A	2/17/87
7082 C	3/23/87
7097B-F	4/07/87
7098A-D	4/08/87
7104A,B	4/14/87
7117A	4/27/87
7167A-D	6/16/87

12. Other test wafers, termed "ECD512" or "512ECD" wafers, were processed by coating and patterning ferroelectric material thereon, starting on April 8, 1987, as indicated by Film IDs 7098E-7100B.

The wafers associated with these Film IDs were silicon wafers that were etched by Orbit Semiconductor, Inc., to form a topography similar to other wafers to be later fabricated with CMOS memory circuits. These initial test wafers were processed through the Krysalis ferroelectric processes as trial runs in preparation for the more expensive ECD512 wafers which had the CMOS memory circuits. As noted in the log, these test wafers were processed with different parameters to determine the results. For example, wafer 7098G had a silicon dioxide layer over which the ferroelectric material was spun. Wafers 7099A-7105B had silicon nitride layers, but some wafers had different types

and layers of bottom electrode materials, processed at different temperatures.

Actual ECD512 wafers with CMOS memory circuits were processed by Krysalis shortly thereafter and are identified in the log as follows:

Film ID	Date Coated
7105C,D	4/15/87
7117B	4/27/87
7125F	5/05/87
7135B,C	5/15/87
7139A	5/19/87
7148A,B	5/28/87
7156A,B	6/05/87
7160A	6/09/87
7162A-D	6/11/87

Like the TD01 CMOS test wafers, the ECD512 CMOS wafers were processed with ferroelectric material layers to form non-volatile memory cells. However, the ECD512 CMOS wafer had many die each with an array of 64x8 memory cells.

13. The ECD512 CMOS wafers were supplied to Krysalis by outside semiconductor vendors who carried out the actual semiconductor processing to form CMOS transistor circuits according to Krysalis specifications. The ECD512 CMOS wafers were subsequently processed by Krysalis personnel, either by myself, or others under my supervision and control, to deposit and pattern the ferroelectric sol-gel material to form a pair of ferroelectric capacitors in association with each memory cell. The patterning of the ferroelectric material to form the individual capacitor dielectric areas on the wafer was carried out using masks that were made by outside vendors according to Krysalis specifications.

14. I conducted numerous experiments and tests while at Krysalis with different compositions of ferroelectric materials to determine if they could be deposited and adhered to different types of bottom electrode conductor materials formed on semiconductor wafers, to determine if the ferroelectric material would be compatible with semiconductor wafer processing techniques, and if the ferroelectric material would operate satisfactorily over long periods of time with acceptable levels of fatigue and aging.

15. Among the number of Krysalis tests conducted with ferroelectric material, there is shown in the log Film IDs 7030A,B which had a thermal silicon dioxide grown over the surface of the silicon wafer, but with no bottom electrode material. The ferroelectric material was applied to the wafer on January 30, 1987. With respect to wafer 7030B, two different compositions, and thus two different layers of ferroelectric material were applied on the same wafer. Two coats of one type of ferroelectric material was applied directly over the silicon dioxide surface, with six coats of a different ferroelectric material thereover. It is believed that tests were conducted to determine if lead would diffuse into the silicon dioxide material during the sintering operation. Also, because the bottom two coats of the ferroelectric material had no zirconium, tests were carried out to determine if the cracking of the ferroelectric material during the sintering operation was alleviated.

16. Also on January 30, 1987, wafer 7030D was coated with eight layers of a particular type of ferroelectric material, and the wafer was annealed after the top electrode deposition. The annealing was carried out at about 400°C to

determine if a better bond could be obtained between the top electrode material and the ferroelectrode material.

17. During February 4 and 5, 1987, wafer 7035A-7035C and 7036A-7036D were processed with a first bottom layer of ferroelectric material, and seven layers of a different ferroelectric material thereover. It was found that the G6307 ferroelectric material exhibits less cracking during the sintering operation, when deposited over silicon dioxide. Also as noted, the different compositions of ferroelectric material included 8/40/60; 15/0/100; 3/60/40; and 0/50/50. Also, some of the wafers had a bottom electrode, and some had the ferroelectric material deposited directly on the silicon dioxide.

18. On February 6, 1987, wafers 7037A, B and C were prepared with composite layers of ferroelectric material on different thicknesses of a spin-on oxide. For example, wafer 7037A had a thousand angstrom titanium layer formed on the silicon wafer, with the composite layers of ferroelectric material deposited thereover. On wafer 7037B, the titanium layer was removed, and thus the ferroelectric composite layer was deposited directly on the spin-on oxide. With wafer 7037C, only 500 angstroms of titanium were deposited on the spin-on oxide. Wafer 7037D was a control wafer, in which a thousand angstroms of titanium was formed on the spin-on oxide, but only a single type, rather than a composite layer, of ferroelectric material was utilized.

19. Wafer 7037E was a wafer obtained from Orbit Semiconductor and cut into quarters for processing according to different tests. One quarter of the wafer had silicon nitride formed on a silicon dioxide, and a "209" oxide formed over the nitride. Wafer 7037F was processed

similarly, except that it underwent a hydrogen fluoride dip. Wafer 7037G was similarly processed, but with two coats of the 209 oxide over the silicon nitride. Wafer 7038A was also similarly processed, but with one type of ferroelectric material rather than a composite material layer. These wafers obtained from Orbit were believed to have been etched to provide a specified topography which was used as a parameter during the wafer processing tests. Also, some of the wafers underwent a sintering operation, while others did not.

20. Other examples of wafer tests include film ID 7043B which was a TD01 CMOS test wafer processed with a single composition of ferroelectric material on February 12, 1987. This wafer had a thin titanium layer over the wafer silicon dioxide, with no capacitor bottom electrode.

21. On February 13, 1987, wafer 7044A, which was a CMOS transistor type of wafer, was processed with a standard bottom electrode material, covered with an 8/40/60 composition of ferroelectric material. The wafer was then cut into 1" squares for lift-off dot mask (LODM) tests. Also, wafer 7044B included a standard bottom electrode material, covered with 250 angstroms of titanium and 1500 angstroms of platinum. Many other wafers were prepared on February 13, 1987, as noted in the log.

22. On February 17, 1987, wafer 7048A was prepared with a composition of ferroelectric material, but rather than sintering in an oxygen ambient, such wafer was both annealed in an argon gas, as well as sintered in an argon gas.

23. On February 25, 1987, wafer 7056A-1 was prepared with a ferroelectric material and annealed immediately after coating thereof.

24. On February 25, 1987, wafer 7056A-1 was dipped in a nitric acid after annealing to roughen the surface to determine if a better adhesion of the ferroelectric material was achieved.

25. Wafer 7056A-2 was prepared with a ferroelectric material on February 25, 1987, and annealed for 72 hours.

26. Wafer 7056A-3 was prepared with a ferroelectric material and a top electrode, and then subjected to an R10 resist stripper and then annealed. This test is believed to be carried out to determine the adhesion capability of the top electrode material following the application of the resist stripper thereto. The resist stripper is utilized in patterning the ferroelectric material. 7056A-4 was similarly processed, but the wafer was soaked in the R10 resist stripping solution for twice the amount of time.

27. Wafer 7056A-6 was prepared with eight coats of a ferroelectric material and then subjected to an acetone and isopropanol solution, and then immediately annealed.

28. On February 25, 1987, wafer 7056A-7 was also prepared with eight coats of a ferroelectric material, and subjected to another type of stripper, denoted "130".

29. On February 25, 1987, wafer 7056A-8 was tested as to a top electrode, by use of a spin-on platinum material.

30. On February 28, 1987, wafer 7059A was prepared with eight coats of an 8/40/60 ferroelectric material and tested with isopropanol supplied by Alfa. I recall that one lot of isopropanol from that supplier caused the synthesis of a sol-gel to be ruined, and thus the present test was to test a new lot of isopropanol on a new sol-gel ferroelectric material.

31. Wafer 7069A was coated with a ferroelectric material on March 10, 1987, to conduct a test of a new top electrode technique, termed "Fat1". With the Fat1 wafer structures, both the top electrode and the bottom electrode of the ferroelectric capacitor were accessible for tests, whereas in the LODM structure, two ferroelectric capacitors were formed in series, with only the outer terminals being accessible, and the inner common terminal was not accessible for testing.

On March 16, 1987, wafer 7075C was prepared with a ferroelectric composition, but not sintered. Other wafers were prepared on such date but sintered at 650°C. The sintered and unsintered wafers were utilized by Krysalis to align and adjust a new semiconductor processing stepper machine purchased from ASM. Such a stepper utilized a laser for aligning the masks to the wafer. The sintered and unsintered wafers exhibited different crystal structures and thus different indices of refraction for aligning the stepper.

32. As noted on page 14 of the log, during March 16, 17 and 18, 1987, numerous different types of ferroelectric compositions, including 3/40/60; 0/50/50; 15/0/100; and 3/60/40 were utilized as different parameters to determine performance characteristics.

33. On March 23, 1987, wafer 7082A was processed with different layers of ferroelectric material to determine which composition exhibited the least cracking during high temperature processing. Particularly, a 15/0/100 composition of ferroelectric material was deposited and then thereover an 8/40/60 composition of ferroelectric material. Such tests were conducted on Orbit test wafers, as well as CMOS wafers, and on both the LODM and Fat1 top electrode structures.

34. On March 27, 1987, wafer 7086A was prepared with a blend of ferroelectric materials. In these tests, the ferroelectric sol-gels were actually mixed together in liquid form to arrive at a composite resultant ferroelectric material.

35. On March 30, 1987, and April 3, 1987, wafers 7089B and 7093A,B were prepared respectively with ferroelectric compositions to conduct a top electrode barrier study. According to this study, efforts were expended to eliminate reactions of aluminum contacts with platinum. It was found that by depositing a titanium layer over the platinum, and then aluminum over the titanium, the adverse material reaction between aluminum and platinum was reduced.

36. On April 4, 1987, a number of wafers were prepared, starting with wafer 7094A to conduct a scratch protection study. In this study, experiments were conducted to select a top passivation layer for covering the ferroelectric capacitors. It is believed that different spin-on glasses, silox and other depositions of materials were used as the passivation layer. As can be seen on the bottom of page 15 of the log, different ramp-in/out parameters were utilized to determine optimum results. In

other words, the speed at which the wafers were fed on a conveyor into the diffusion furnace was varied to vary the temperature gradient to which the wafers were exposed. Many materials adversely react with the ferroelectric material, and thus the selection of a passivation layer was significant in fabricating ferroelectric memories. Not only do various materials chemically react with ferroelectric material, but such materials can also place a mechanical stress on the ferroelectric material. Because the ferroelectric material exhibits piezoelectric properties, external stresses can change the characteristics of the ferroelectric material.

37. On April 6, 1987, wafers 7096C and D were prepared with an 8/40/60 composition of ferroelectric material, but with different amounts of excess lead. These wafers were prepared to conduct an excess lead study. As noted in the FES coating log, wafer 7096C was prepared with a ferroelectric material having no excess lead, while wafer 7096D was prepared having 30 parts of excess lead.

38. On April 7 and 8, 1987, a number of TD01 CMOS wafers were prepared with different compositions of ferroelectric material, as well as other different parameters, to conduct pre-512 process tune-up. The TD01 CMOS wafers were processed through the Krysalis processing equipment to determine the correct operation thereof before processing the more expensive ECD512 CMOS wafers. The TD01 CMOS wafers are identified at pages 16 and 17 of the log, starting with wafer 7097B.

39. On April 8, 1987, a number of ECD512 test wafers were prepared, starting with 7098E. These test wafers had no CMOS memory circuits, but underwent a pre-etch to provide a topography similar to a ECD512 wafer with CMOS memory circuits. The ECD512 test wafers bearing film IDs 7098E-7100B were processed with different parameters, such as some having eight coats of ferroelectric material, while wafer 7098G had 32 coats. Also, the ferroelectric material on some of the wafers was deposited over a single spin-on layer of titanium, while other wafers had the ferroelectric material deposited over two such layers of the titanium material. In addition, some wafers underwent an oxidation cycle at 650°C, while others were subjected to an oxidizing environment of 750°C.

40. ECD512A wafers 7105A,D were prepared on April 15, 1987, with a ferroelectric material. These wafers were fabricated at Orbit Semiconductor with CMOS memory transistors and circuits.

41. On April 16, 1987, wafers 7106C, D and E were prepared with different ferroelectric compositions for test evaluation purposes. Particularly, wafer 7106C had a blend of G7072 and G7090A ferroelectric material, yielding a 5.5/40/60,+5 resulting composition. Wafer 7106D was prepared with a 50:50 blend of G7072 and G7055 ferroelectric material, resulting in a composition of 5.5/40/60,+10. Wafer 7106E was prepared with a 1/2:1/6:1/3 blend of G7072 and 7090A and 7091 ferroelectric sol-gels which resulted in a 5.5/40/60,+15 resultant blend. The excess lead compositions for each of the blends differed, thus providing materials for evaluating with respect to ferroelectric properties.

42. On April 24, 1987, yet other wafers were prepared, starting with wafer 7114A to conduct a bottom electrode study. In this study, different thicknesses of titanium dioxide were deposited under the bottom electrode which comprised 500 angstroms of titanium and 1000 angstroms of platinum.

43. On April 27, 1987, TD01 CMOS wafer 7117A was processed with a layer of ferroelectric material for conducting yet another bottom electrode study. On the same date, an ECD512 wafer with CMOS memory circuits (7117B) was processed with a layer of ferroelectric material, to also conduct a bottom electrode test.

44. On April 30, 1987, wafers 7120B-D were prepared with the same composition of ferroelectric material to conduct an interlevel dielectric (ILD) study. The interlayer dielectric comprised a spin-on oxide deposited over the top electrode of the ferroelectric capacitor.

45. On May 1, 1987, wafers 7121A-C were prepared with a composition of ferroelectric materials to conduct a buffer layer study. Two different ferroelectric sol-gels were deposited in different layers with an intermediate buffer layer to determine the extent of blistering after the sintering operation.

46. On May 5, 1987, wafers 7125A and B were processed with ferroelectric material, but were not annealed, to conduct tests for aligning the wafer processing stepper equipment.

47. On May 5, 1987, ECD512A wafer 7125F was prepared with eight coats of a ferroelectric material to conduct tests on the non-volatile ferroelectric memory cells.

48. On May 11, 1987, a Fatl wafer (7131A) was prepared with eight coats of a ferroelectric composition 3/60/40 to conduct fatigue tests thereon.

49. On May 12, 1987, wafer 7132A was prepared with a ferroelectric material to conduct ion gun etch studies. This evaluation was to determine the effect of ion etching on ferroelectric material, rather than the standard use of wet etching solutions.

50. On May 15, 1987, ECD512A wafers 7135B,C and 7139A were prepared with ferroelectric compositions, and thereafter tested to determine the electrical characteristics of the non-volatile memory cells.

51. On May 22, 1987, wafers 7142A,B were prepared with a new sol-gel ferroelectric composition, defined as 0/50/50,+10.

52. On May 28, 1987, ECD512A wafers having CMOS memory circuits, identified as film IDs 7148A,B, were prepared with different ferroelectric materials to be evaluated accordingly.

53. On June 1, 1987, wafer 7152A was prepared with compositions of ferroelectric materials having buffer layers therebetween. On the same day, wafers 7152C and D were processed with ferroelectric materials to conduct a film thinness study.

54. On June 4, 1987, wafers 7155A-C were prepared with new compositions of ferroelectric material, namely 0/50/50; 1/45/55 and 0/40/60 to conduct electrical tests of the ferroelectric material.

55. As noted on pages 20-28 of the FES coating log, many other wafers were prepared with ferroelectric materials for conducting tests subsequent to June 5, 1987.

56. Exhibit B is a copy of my memorandum dated June 16, 1987, concerning failure rate studies of numerous chips, or die, cut from the CMOS ECD512A wafer identified as Film ID 7148A. As noted in the log of Exhibit A, such wafer was processed with a ferroelectric material on May 28, 1987, and tested by Mr. David Eaton, also a Krysalis employee, who provided the bit failures of six of the die cut from the wafer.

57. On information and belief, electrical tests on the wafers noted above were actually carried out by Krysalis personnel.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable

by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: June 28, 1991

Leo N. Chapin

Leo N. Chapin

FILM ID	DATE COATED	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL TYPE
F6060				G, (),	cts @ rpm				
F6107	08/02/86	Si 1/4 Wafer 10min-625°C anneal. .	B10	G6192, (8/40/60,+10), 22	10cts @ 2000rpm		NA	550°sinter	?
F6109	08/02/86	Si 1/4 Wafer 10min-625°C anneal. .	B10	G6208, (8/40/60,+10), 6	10cts @ 2000rpm		NA	550°sinter	?
F6110	08/02/86	Pt#10 10min-625°C anneal. .	Pt#10	G6210, (3/40/60,+10), 4	10cts @ 2000rpm		NA	550°sinter	?
F6111	08/02/86	Pd#1 10min-625°C anneal. .	Pd#1	G6210, (3/40/60,+10), 4	10cts @ 2000rpm		NA	550°sinter	?
F6113	08/02/86	Si Wafer 10min-625°C anneal. .	B10	G6210, (3/40/60,+10), 4	10cts @ 2000rpm		NA	550°sinter	?
F6115	08/02/86	Si 1/4 Wafer 10min-625°C anneal. .	B10	G6213, (3/60/40,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
F6117	08/06/86	Si 1/4 Wafer 120min-625°C anneal. .	B10	G6208, (8/40/60,+10), 10	10cts @ 2000rpm		NA	550°sinter	?
F6119	08/06/86	Si 1/4 Wafer 120min-625°C anneal. .	B10	G6210, (3/40/60,+10), 8	10cts @ 2000rpm		NA	550°sinter	?
F6120	08/06/86	Si 1/4 Wafer 120min-625°C anneal. .	B10	G6213, (3/60/40,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
F6121	08/12/86	Si 1/4 Wafer 10min-625°C anneal. .	B11	G6208, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
F6122	08/12/86	Si 1/4 Wafer 10min-625°C anneal. .	B11	G6210, (3/40/60,+10), 14	10cts @ 2000rpm		NA	550°sinter	?
F6123	08/12/86	Si 1/4 Wafer 10min-625°C anneal. .	B11	G6213, (3/60/40,+10), 11	10cts @ 2000rpm		NA	550°sinter	?
F6124	08/12/86	Si 1/4 Wafer 30min-625°C anneal. .	B11	G6208, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
F6127	08/12/86	Si 1/4 Wafer 30min-625°C anneal. .	B11	G6213, (3/60/40,+10), 11	10cts @ 2000rpm		NA	550°sinter	?
F6128	08/12/86	Si 1/4 Wafer 30min-600°C anneal. .	B11	G6208, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
F6129	08/12/86	Si 1/4 Wafer 30min-600°C anneal. .	B11	G6210, (3/40/60,+10), 14	10cts @ 2000rpm		NA	550°sinter	?
F6130	08/12/86	Si 1/4 Wafer 30min-600°C anneal. .	B11	G6213, (3/60/40,+10), 11	10cts @ 2000rpm		NA	550°sinter	?
F6131	08/12/86	Si 1/4 Wafer 60min-600°C anneal. .	B11	G6208, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
F6132	08/12/86	Si 1/4 Wafer 60min-600°C anneal. .	B11	G6210, (3/40/60,+10), 14	10cts @ 2000rpm		NA	550°sinter	?
F6134	08/12/86	Si 1/4 Wafer 60min-600°C anneal. .	B11	G6213, (3/60/40,+10), 11	10cts @ 2000rpm		NA	550°sinter	?
F6135	08/15/86	Si Wafer 30min-625°C anneal. .	B10	G6213, (3/60/40,+10), 14	10cts @ 2000rpm		NA	550°sinter	?
F6136	08/21/86	Pt#12	Pt#12	G6208, (8/40/60,+10), 25	10cts @ 2000rpm		NA	550°sinter	?

FILM ID	DATE COATED	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL TYPE
F6137	08/27/86	1/4wafer	B10or11	G6208, (8/40/60,+10),	12cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6208 is old CODE G620.								
F6138	08/28/86	1/4wafer	B10or11	G6208, (8/40/60,+10),	8cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6208 is old CODE G620.								
F6139	08/28/86	1/4wafer	B10or11	G6208, (8/40/60,+10),	6cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6208 is old CODE G620.								
F6140	08/27/86	Pt#1	Pt#1	G6208, (8/40/60,+10),	10cts @ 2000rpm		NA	550°sinter	?
	60min-600°C anneal. G6208 is old CODE G620.								
F6141	08/27/86	Pt#3	Pt#3	G6208, (8/40/60,+10),	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6220B	08/08/86	Si Wafer	B11	G6208, (8/40/60,+10),	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6247A	09/04/86	Si Wafer	B19	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247B	09/04/86	Si Wafer	B17	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247C	09/04/86	Si Wafer	B17	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247D	09/04/86	Si Wafer	B18	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247E	09/04/86	Si Wafer	B18-patt	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247F	09/04/86	Si Wafer	B17-patt	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247G	09/04/86	Si Wafer	B17-patt	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247H	09/04/86	Si Wafer	B17-patt	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247I	09/04/86	Si Wafer	B17-patt	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247J	09/04/86	Si Wafer	B17-patt	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247K	09/04/86	Si Wafer	B18-patt	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6247L	09/04/86	Si Wafer	B18-patt	G6208, (8/40/60,+10), 39	10cts @ 2000rpm		NA	550°sinter	?
	30min-625°C anneal. G6208 is old CODE G620.								
6248A	09/05/86	Si Wafer	B19	G6208, (8/40/60,+10), 40	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6208 is old CODE G620.								
6248B	09/05/86	Si Wafer	B17	G6210, (3/40/60,+10), 38	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6210 is old CODE G621.								
6248D	09/05/86	Si Wafer	B19-patt	G6208, (8/40/60,+10), 40	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,10"/min ramp. G6208 is old CODE G620.								
6252A	09/09/86	Si Wafer	B20	G6208, (8/40/60,+10), 44	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6208 is old CODE G620.								
6252B	09/09/86	Si Wafer	B16-patt	G6208, (8/40/60,+10), 44	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6208 is old CODE G620.								

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6252C	09/09/86	Si Wafer	B16-patt	G6208, (8/40/60,+10), 44	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6208 is old CODE G620.								
6252D	09/09/86	Si Wafer	B20-patt	G6208, (8/40/60,+10), 44	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6208 is old CODE G620.								
6252E	09/09/86	Si Wafer	B20	G6251, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6251 is old CODE G623.								
6252F	09/09/86	Si Wafer	B20-patt	G6251, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6251 is old CODE G623.								
6252G	09/09/86	Si Wafer	B16	G6210, (3/40/60,+10), 42	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6210 is old CODE G621.								
6252H	09/09/86	Si Wafer	B21	G6210, (3/40/60,+10), 42	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6210 is old CODE G621.								
6252I	09/09/86	Si Wafer	B21-patt	G6210, (3/40/60,+10), 42	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal. G6210 is old CODE G621.								
6252J	09/09/86	Si Wafer	B16	G6251, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,10"/min ramp. G6251 is old CODE G623.								
6254A	09/11/86	Si Wafer	B22-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,10"/min ramp;control for 6254F. G6208 is old CODE G620.								
6254B	09/11/86	Si Wafer	B22-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,10"/min ramp;control for 6254F. G6208 is old CODE G620.								
6254C	09/11/86	Si Wafer	B22-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,5"/min ramp. G6208 is old CODE G620.								
6254D	09/11/86	Si Wafer	B22-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,5"/min ramp. G6208 is old CODE G620.								
6254E	09/11/86	Si Wafer	B22-patt	G6210, (3/40/60,+10), 44	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,5"/min ramp. G6210 is old CODE G621.								
6254F	09/11/86	Si Wafer	B22-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,10"/min ramp;EDTA-H2O2 clean. G6208 is old CODE G620.								
6254G	09/11/86	Si Wafer	B22-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,5"/min ramp;EDTA-H2O2 clean. G6208 is old CODE G620.								
6254H	09/11/86	Si Wafer	B22-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,5"/min ramp;EDTA-H2O2 clean. G6208 is old CODE G620.								
6254I	09/11/86	Si Wafer	B22-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,5"/min ramp;EDTA-H2O2 clean. G6208 is old CODE G620.								
6254J	09/11/86	Si Wafer	B21-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,5"/min ramp. G6208 is old CODE G620.								
6254K	09/11/86	Si Wafer	B19-patt	G6208, (8/40/60,+10), 46	10cts @ 2000rpm		NA	550°sinter	?
	30min-600°C anneal,10"/min ramp;EDTA-H2O2 clean. G6208 is old CODE G620.								
6255A	09/12/86	Si Wafer	B23-patt	G6208, (),	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal,10"/min ramp. .								
6255B	09/12/86	Si Wafer	B23-patt	G6208, (),	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal,10"/min ramp. .								
6255C	09/12/86	Si Wafer	B23-patt	G6251, (),	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal,10"/min ramp. .								
6255D	09/12/86	Si Wafer	B23-patt	G6251, (),	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal,10"/min ramp. .								

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6255E	09/12/86	Si Wafer	B23-patt	G6251, (),	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp. .								
6258A	09/15/86	Si Wafer	B25-patt	G6208, (8/40/60,+10), 58	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp. .								
6258B	09/15/86	Si Wafer	B25-patt	G6208, (8/40/60,+10), 58	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp. .								
6258C	09/15/86	Si Wafer	B23-patt	G6208, (8/40/60,+10), 58	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp. .								
6258D	09/15/86	Si Wafer	B25-patt	G6251, (8/40/60,+10), 7	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp. .								
6258F	09/15/86	Si Wafer	B23-patt	G6251, (8/40/60,+10), 7	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp. .								
6258G	09/15/86	Si Wafer	B25-patt	G6251, (8/40/60,+10), 7	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp. .								
6260A	09/17/86	Si Wafer	B25-patt	G6251, (8/40/60,+10), 9	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp;control. .								
6260B	09/17/86	Si Wafer	B26-patt	G6251, (8/40/60,+10), 9	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp;control. .								
6260C	09/17/86	Si Wafer	B26-patt	G6251, (8/40/60,+10), 9	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp;EDTA-H2O2 clean. .								
6260D	09/17/86	Si Wafer	B26-patt	G6251, (8/40/60,+10), 9	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp;EDTA-H2O2 clean. .								
6260E	09/17/86	Si Wafer	B26-patt	G6251, (8/40/60,+10), 9	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp;EDTA-H2O2 clean. .								
6260F	09/17/86	Si Wafer	B26-patt	G6251, (8/40/60,+10), 9	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp;EDTA-H2O2 clean. .								
6260G	09/17/86	Si Wafer	B25-patt	G6251, (8/40/60,+10), 9	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal,10°/min ramp;EDTA-H2O2 clean. .								
6260H	09/17/86	TiNitride	None	G6251, (8/40/60,+10), 9	1cts @ 2000rpm		NA	550°sinter	?
	Blistered and cracked after 1st coat sinter. .								
6261A	09/18/86	Si Wafer	B25,5-55p	G6210, (3/40/60,+10), 51	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal. .								
6261B	09/18/86	Si Wafer	B25,6-55p	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal. .								
6261C	09/18/86	Si Wafer	B26,1-60p	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal. .								
6261D	09/18/86	Si Wafer	B26,2-70p	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal. .								
6261E	09/18/86	Si Wafer	B26,4-60p	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal. .								
6261F	09/18/86	Si Wafer	B27,2patt	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal. .								
6261G	09/18/86	Si Wafer	B27,3patt	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal. .								
6261H	09/18/86	Si Wafer	B27,4patt	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÀC anneal. .								

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6261I	09/18/86	Si Wafer	B27,5patt	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6261J	09/18/86	Si Wafer	B27,6patt	G6251, (8/40/60,+10), 10	8cts @ 2000rpm		NA	550°sinter	?
	No anneal. .								
6261K	09/18/86	Si Wafer	B25,3-65p	G6255, (10/40/60,+10), 6	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267A	09/24/86	OrbNitride	1/4B28	G6251, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267B	09/24/86	OrbNitride	1/4B28pat	G6251, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267C	09/24/86	OrbNitride	1/4B28pat	G6251, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267D	09/24/86	2"CVD Nit	B28patt	G6251, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267E	09/24/86	2"CVD Nit	B28patt	G6251, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267F	09/24/86	2"CVD Nit	B28patt	G6251, (8/40/60,+10), 16	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267G	09/24/86	2"CVD Nit	B28patt	G6255, (10/40/60,+10), 12	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267H	09/24/86	2"CVD Nit	B28patt	G6253, (6/40/60,+10), 14	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267I	09/24/86	2"Oxide	B28patt	G6253, (6/40/60,+10), 14	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6267J	09/24/86	2"Oxide	B28patt	G6253, (6/40/60,+10), 14	10cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6272A	09/29/86	Si Wafer	B23	G6251, (8/40/60,+10), 21	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6272B	09/29/86	Si Wafer	B23	G6251, (8/40/60,+10), 21	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6272C	09/29/86	Si Wafer	B27	G6251, (8/40/60,+10), 21	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6272D	09/29/86	Si Wafer	B27	G6251, (8/40/60,+10), 21	8cts @ 2000rpm		NA	550°sinter	?
	30min-600ÅC anneal. .								
6273A	09/30/86	Si Wafer	B17	G6251, (8/40/60,+10), 22	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6273B	09/30/86	Si Wafer	B19	G6251, (8/40/60,+10), 22	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6273C	09/30/86	Si Wafer	B21	G6251, (8/40/60,+10), 22	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6273D	09/30/86	Si Wafer	B27	G6251, (8/40/60,+10), 22	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6273E	09/30/86	Si Wafer	B27rnd	G6251, (8/40/60,+10), 22	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6276A	10/03/86	Si Wafer,sqr	B29	G6251, (8/40/60,+10), 25	10cts @ 2000rpm		NA	550°sinter	?
	. .								

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6276B	10/03/86	Si Wafer	B29flat	G6251, (8/40/60,+10), 25	10cts @ 2000rpm		NA	550°sinter	?
6276C	10/03/86	Si Wafer	B29rnd	G6251, (8/40/60,+10), 25	10cts @ 2000rpm		NA	550°sinter	?
6276D	10/03/86	Si Wafer	B29rnd	G6251, (8/40/60,+10), 25	10cts @ 2000rpm		NA	550°sinter	?
6276E	10/03/86	Pt#5	Pt#5	G6251, (8/40/60,+10), 25	10cts @ 2000rpm		NA	550°sinter	?
6279A	10/06/86	Si Wafer	B29flat	G6208, (8/40/60,+10), 71	10cts @ 2000rpm		NA	550°sinter	?
6279B	10/06/86	Si Wafer	B29rnd	G6208, (8/40/60,+10), 71	10cts @ 2000rpm		NA	550°sinter	?
6280A	10/07/86	Si Wafer	B29rnd	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6280B	10/07/86	Si 1/4 Wafer	B30-1,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6280C	10/07/86	Si 1/4 Wafer	B30-2,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6280D	10/07/86	Si 1/4 Wafer	B30-3,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6280E	10/07/86	Si 1/4 Wafer	B30-4,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6280F	10/07/86	Si 1/4 Wafer	B30-5,LR	G6279, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6281A	10/08/86	Si Wafer	B29rnd	G6279, (8/40/60,+10), 2	10cts @ 2000rpm		NA	500°sinter	?
	Low temp sinter - 500°C. .								
6282A	10/09/86	Si Wafer	B29rnd	G6279, (8/40/60,+10), 3	10cts @ 2000rpm		NA	450°sinter	?
	Anneal 1/4 30min-500°C, 1/4 30min-550°C;10°/min ramp. .								
6285A	10/13/86	Si 1/4 Wafer	B30-1,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		NA	550°sinter	?
6285B	10/13/86	Si 1/4 Wafer	B30-2,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		NA	550°sinter	?
6285C	10/13/86	Si 1/4 Wafer	B30-3,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		NA	550°sinter	?
6285D	10/13/86	Si 1/4 Wafer	B30-4,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		NA	550°sinter	?
6285E	10/13/86	Si 1/4 Wafer	B30-5,LL	G6279, (8/40/60,+10), 6	10cts @ 2000rpm		NA	550°sinter	?
6286A	10/14/86	Si 1/4 Wafer	B30-1,UL	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		NA	550°sinter	?
6286B	10/14/86	Si 1/4 Wafer	B30-1,UR	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		NA	550°sinter	?
6286C	10/14/86	Si 1/4 Wafer	B30-2,UL	G6279, (8/40/60,+10), 7	3cts @ 2000rpm		NA	550°sinter	?
6286D	10/14/86	Si 1/4 Wafer	B30-2,UR	G6279, (8/40/60,+10), 7	3cts @ 2000rpm		NA	550°sinter	?

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6286E	10/14/86	Si 1/4 Wafer	B30-3,UL	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		NA	550°sinter	?
6286F	10/14/86	Si 1/4 Wafer	B30-3,UR	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		NA	550°sinter	?
6286G	10/14/86	Si 1/4 Wafer	B30-4,UL	G6279, (8/40/60,+10), 7	3cts @ 2000rpm		NA	550°sinter	?
6286H	10/14/86	Si 1/4 Wafer	B30-4,UR	G6279, (8/40/60,+10), 7	3cts @ 2000rpm		NA	550°sinter	?
6286I	10/14/86	Si 1/4 Wafer	B30-5,UL	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		NA	550°sinter	?
6286J	10/14/86	Si 1/4 Wafer	B30-5,UR	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		NA	550°sinter	?
6286K	10/14/86	Pt#6	Pt#6	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		NA	550°sinter	?
6286L	10/14/86	Pt#7	Pt#7	G6279, (8/40/60,+10), 7	10cts @ 2000rpm		NA	550°sinter	?
6287A	10/15/86	Si 1/4 Wafer	B30-3,UR	G6208, (8/40/60,+10), 79	10cts @ 2000rpm		NA	550°sinter	?
6288A	10/16/86	Si 1/4 Wafer	B32-1,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6288B	10/16/86	Si 1/4 Wafer	B32-1,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6288C	10/16/86	Si 1/4 Wafer	B32-2,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6288D	10/16/86	Si 1/4 Wafer	B32-2,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6288E	10/16/86	Si 1/4 Wafer	B32-3,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6288F	10/16/86	Si 1/4 Wafer	B32-3,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6288G	10/16/86	Si 1/4 Wafer	B32-4,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6288H	10/16/86	Si 1/4 Wafer	B32-4,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6288I	10/16/86	Si 1/4 Wafer	B32-5,LL	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6288J	10/16/86	Si 1/4 Wafer	B32-5,LR	G6279, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	?
6293A	10/21/86	Pt#9	Pt#9	G6292, (0/50/50,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6293B	10/21/86	Pt#14	Pt#14	G6292, (0/50/50,+10), 1	20cts @ 2000rpm		NA	550°sinter	?
6293C	10/21/86	Pt#17	Pt#17	G6292, (0/50/50,+10), 1	20cts @ 2000rpm		NA	550°sinter	?
6293D	10/21/86	Si Wafer	Pt on Si	G6292, (0/50/50,+10), 1	5cts @ 2000rpm		NA	550°sinter	?

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6294A	10/22/86	Si Wafer	B29rnd	G6292, (0/50/50,+10), 2	7cts @ 2000rpm		NA	550°sinter	?
6296A	10/24/86	Si Wafer	B35-3/0	G6279, (8/40/60,+10), 17	10cts @ 2000rpm		NA	550°sinter	?
6296B	10/24/86	Si Wafer	B35-4/0	G6279, (8/40/60,+10), 17	10cts @ 2000rpm		NA	550°sinter	?
6296C	10/24/86	Si 1/4 Wafer	B35-1,LL	G6279, (8/40/60,+10), 17	10cts @ 2000rpm		NA	550°sinter	?
6296D	10/24/86	Si 1/4 Wafer	B35-2,LL	G6279, (8/40/60,+10), 17	10cts @ 2000rpm		NA	550°sinter	?
6297A				G, (),	cts @ rpm				
6297B				G, (),	cts @ rpm				
6300A	10/27/86	Si 1/4 Wafer	B33-1	G6292, (0/50/50,+10), 8	10cts @ 2000rpm		NA	550°sinter	?
6300B	10/27/86	Si 1/4 Wafer	B33-2patt	G6292, (0/50/50,+10), 8	10cts @ 2000rpm		NA	550°sinter	?
6300C	10/27/86	Si 1/4 Wafer	B33-3patt	G6292, (0/50/50,+10), 8	8cts @ 2000rpm		NA	550°sinter	?
6300D	10/27/86	Si 1/4 Wafer	B33-5patt	G6292, (0/50/50,+10), 8	10cts @ 2000rpm		NA	550°sinter	?
6301A	10/28/86	Si Wafer	B34-4	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6301B	10/28/86	Si Wafer	B34-1	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6301C	10/28/86	Si Wafer	B34-2	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6301D	10/28/86	Si Wafer	B34-3	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6301E	10/28/86	Si Wafer	B34-5	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6301F	10/28/86	Si 1/4 Wafer	B35-1,UR	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6301G	10/28/86	Si 1/4 Wafer	B35-1,UL	G6300, (8/40/60,+10), 1	10cts @ 2000rpm		NA	550°sinter	?
6301H	10/28/86	Si 1/4 Wafer	B32-1,UR	G6279POLY, (8/40/60,+10), 22	10cts @ 2000rpm		NA	550°sinter	?
6305A	11/01/86	Si 1/4 Wafer	B35-1,LR	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
6305B	11/01/86	Si 1/4 Wafer	B35-2,LR	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
6305C	11/01/86	Si 1/4 Wafer	B35-3,LL	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
	Oxide - No anneal. .								
6305D	11/01/86	Si 1/4 Wafer	B35-3,UL	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
	Oxide - Annealed - 30min-600°C. .								

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6305E	11/01/86	Si 1/4 Wafer	B35-3,UR	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
	No oxide - Annealed - 30min-600°C. .								
6305F	11/01/86	Si 1/4 Wafer	B35-3,LR	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
	No oxide - No anneal. .								
6305G	11/01/86	Si 1/4 Wafer	B35-4,LL	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
	Oxide - No anneal. .								
6305H	11/01/86	Si 1/4 Wafer	B35-4,UL	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
	Oxide - Annealed - 30min-600°C. .								
6305I	11/01/86	Si 1/4 Wafer	B35-4,UR	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
	No oxide - Annealed - 30min-600°C. .								
6305J	11/01/86	Si 1/4 Wafer	B35-4,LR	G6300, (8/40/60,+10), 5	10cts @ 2000rpm		NA	550°sinter	?
	No oxide - No anneal. .								
6309A	11/05/86	OrbTW	?	G6300, (8/40/60,+10), 9	10cts @ 2000rpm		NA	550°sinter	TDO1
	. .								
6310A	11/06/86	OrbTD01cmos	?	G6300, (8/40/60,+10), 10	10cts @ 2000rpm		NA	550°sinter	TDO1
	"Adeline". .								
6311A	11/07/86	Pt#16	Pt#16	G6307, (15/0/100,+10), 4	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6311B	11/07/86	Si Wafer	B20	G6307, (15/0/100,+10), 4	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6315A	11/13/86	OrbTW	?	G6279, (8/40/60,+10), 36	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6315B	11/13/86	OrbTD01cmos	?	G6279, (8/40/60,+10), 36	10cts @ 2000rpm		NA	550°sinter	?
	"Beaulah". .								
6324A	11/20/86	Pd#2	Pd#2	G6300, (8/40/60,+10), 24	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6324B	11/20/86	?	?	G6300, (8/40/60,+10), 24	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6324C	11/20/86	?	?	G6300, (8/40/60,+10), 24	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6324D	11/20/86	2" Wafer	?	G6300, (8/40/60,+10), 24	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6324E	11/20/86	Pt#1	Pt#1	G6319, (8/40/60,+0), 5	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6324F	11/20/86	Si 1/4 Wafer	B38-3,LL	G6319, (8/40/60,+0), 5	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6324G	11/20/86	2" Wafer	?	G6319, (8/40/60,+0), 5	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6324H	11/20/86	Pt#3	Pt#3	G6322, (8/0/100,+10), 2	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6324I	11/20/86	Si 1/4 Wafer	B38-3,LR	G6322, (8/0/100,+10), 2	10cts @ 2000rpm		NA	550°sinter	?
	. .								
6332A	11/28/86	CMOS	B39	G6300, (8/40/60,+10), 32	10cts @ rpm		NA	550 sinter	?
	"Erma"; 8/40/60. .								
6335A	12/01/86	CMOS	B40	G6300, (8/40/60,+10), 35	10cts @ rpm		NA	550 sinter	?
	"Fred"; 8/40/60. .								

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6335B	12/01/86 "Ginger"; 8/40/60. .	CMOS	B40	G6300, (8/40/60,+10), 35	10cts @ rpm		NA	550 sinter	?
6337A	12/03/86 "Hector". .	CMOS	B41	G6300, (8/40/60,+10), 37	10cts @ rpm		NA	550 sinter	?
6337B	12/03/86 "Irene". .	CMOS	B41	G6300, (8/40/60,+10), 37	10cts @ rpm		NA	550 sinter	?
6339A	12/05/86 "Joc";0/53/47,+10. .	CMOS	B41	G6292, (0/53/47,+10), 47	10cts @ rpm		NA	550 sinter	?
6339B	12/05/86 "Kitty"; 8/40/60,+10. .	CMOS	B41	G6335, (8/40/60,+10), 4	10cts @ rpm		NA	550 sinter	?
6339D	12/05/86 . .	?	B41	G6335, (8/40/60,+10), 4	10cts @ rpm		NA	550 sinter	?
6339E	12/05/86 . .	?	39/40	G6335, (8/40/60,+10), 4	10cts @ rpm		NA	550 sinter	?
6339F	12/05/86 . .	?	39/40	G6335, (8/40/60,+10), 4	10cts @ rpm		NA	550 sinter	?
6342A	12/08/86 "Leroy". .	CMOS	39/40	G6335, (8/40/60,+10), 7	10cts @ rpm		NA	550 sinter	?
6342B	12/08/86 "Mae". .	CMOS	B42	G6335, (8/40/60,+10), 7	10cts @ rpm		NA	550 sinter	?
6342C	12/08/86 "Nick. .	CMOS	B42	G6335, (8/40/60,+10), 7	10cts @ rpm		NA	550 sinter	?
6342D	12/08/86 "Olga". .	CMOS	B42	G6335, (8/40/60,+10), 7	10cts @ rpm		NA	550 sinter	?
6350A	12/16/86 . .	Si 1/4 Wafer	B39,UR	G6300, (8/40/60,+10), 50	10cts @ 2000rpm		NA	550°sinter	?
6350B	12/16/86 . .	Si 1/4 Wafer	B39,LR	G6335, (8/40/60,+10), 15	10cts @ 2000rpm		NA	550°sinter	?
6351A	12/17/86 . .	Th Oxide	?	G6292, (0/50/50,+10), 59	10cts @ rpm		2@300	30@650inO2	?
6351B	12/17/86 . .	Th Oxide	?	G6335, (8/40/60,+10), 16	10cts @ rpm		2@300	30@650inO2	?
6358E	09/15/86 30min-600ÅC anneal,10°/min ramp. .	Si Wafer	B25-patt	G6251, (8/40/60,+10), 7	8cts @ 2000rpm		NA	550°sinter	?
7014A	01/14/87 0/53/47,+10. .	A1	B42	G6292, (0/53/47,+10), 87	8cts @ rpm		2@400	?	?
7014B	01/14/87 15/0/100,+10. .	A2	B42	G6307, (15/0/100,+10), 72	8cts @ rpm		2@400	?	?
7014C	01/14/87 0/53/47,+10. .	A2	B47-3	G6292, (0/53/47,+10), 87	8cts @ rpm		2@400	?	?
7014D	01/14/87 8/40/60,+10. .	A2	B47-3	G7006A, (8/40/60,+10), 8	8cts @ rpm		2@400	?	?
7014E	01/14/87 15/0/100,+10. .	A2	B47-3	G6307, (15/0/100,+10), 72	8cts @ rpm		2@400	?	?
7015A	01/15/87 15/0/100,+10. .	Oxide	B47-3	G6307, (15/0/100,+10), 73	9cts @ rpm		2@400	?	?

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7015B	01/15/87	Oxide	B47-3	G6322, (8/0/100,+10), 58	9cts @ rpm		2@400	?	?
	8/0/100,+10. .								
7016A	01/16/87	Oxide	B43	G7006A, (8/40/60,+10), 10	8cts @ rpm		2@400	30@650inO2	?
	. .								
7016B	01/16/87	Oxide	B43	G7006A, (8/40/60,+10), 10	8cts @ rpm		2@400	30@650inO2	?
	. .								
7016C	01/16/87	Oxide	B47-5	G6307, (15/0/100,+10), 74	8cts @ rpm		2@400	30@650inO2	?
	. .								
7016D	01/16/87	Oxide	B47-4	G6307, (15/0/100,+10), 74	8cts @ rpm		2@400	30@650inO2	?
	. .								
7021A	01/21/87	Oxide	B47-4	G7006A, (8/40/60,+10), 15	5cts @ rpm		2@400	?	?
	. .								
7021B	01/21/87	Oxide	B47-4	G7006A, (8/40/60,+10), 15	5cts @ rpm		2@400	?	?
	. .								
7021C	01/21/87	Oxide	B47-4	G7006A, (8/40/60,+10), 15	5cts @ rpm		2@400	?	?
	. .								
7023A	01/23/87	Oxide	B49	G7020, (3/60/40,+10), 3	8cts @ 2000rpm		2@400	30@650inO2	?
	3/60/40,+10. .								
7023B	01/23/87	Oxide	B49	G7021, (12/0/100,+10), 2	8cts @ 2000rpm		2@400	30@650inO2	?
	. .								
7023C	01/23/87	Oxide	B49	G7022, (0/50/50,+10), 1	8cts @ 2000rpm		2@400	30@650inO2	?
	. .								
7023D	01/23/87	Oxide	B49	G7006A, (8/40/60,+10), 17	8cts @ 2000rpm		2@400	30@650inO2	?
	. .								
7023E	01/23/87	Oxide	None	G7021, (12/0/100,+10), 2	8cts @ 2000rpm		2@400	30@650inO2	?
	. .								
7023F	01/23/87	Oxide	B49	G7006A, (8/40/60,+10), 17	8cts @ 2000rpm		2@450	30@650inO2	?
	. .								
7023G	01/23/87	Oxide	B49	G7006A, (8/40/60,+10), 17	5cts @ 2000rpm		2@450	30@650inO2	?
	. .								
7023H	01/23/87	Oxide	B49	G7006A, (8/40/60,+10), 17	8cts @ 2000rpm		2@450	30@650inO2	?
	. .								
7028A	01/28/87	Oxide	B49	G6307, (15/0/100,+10), 86	8cts @ rpm		2@400	30@700inO2	?
	15/0/100,+10; Tube#3 settings for 700°C anneal;575,960,665. .								
7028B	01/28/87	Oxide	B49	G7006A, (8/40/60,+10), 22	8cts @ rpm		2@400	30@700inO2	?
	8/40/60,+10; 700°C anneal. .								
7028C	01/28/87	Oxide	B49	G7020, (3/60/40,+10), 8	8cts @ rpm		2@400	30@700inO2	?
	3/60/40,+10; 700°C anneal. .								
7028D	01/28/87	Oxide	B49	G7022, (0/50/50,+10), 6	8cts @ rpm		2@400	30@700inO2	?
	0/50/50,+10; 700°C anneal. .								
7028E	01/28/87	Pt#12	PT	G7006A, (8/40/60,+10), 22	8cts @ rpm		2@400	30@700inO2	LODM
	8/40/60,+10 on bulk Pt; 700°C anneal. .								
7030A	01/30/87	Th Oxide	NONE	G6307, (15/0/100,+10), 88	8cts @ rpm		2@400	30@650inO2	LODM
	Thermal oxide on 2"wafer; control for 7030B. .								
7030B	01/30/87	Th Oxide	NONE	G6307/7006A,	2/6cts @ rpm		2@400	30@650inO2	LODM
	Thermal oxide on 2"wafer; first composite FES on oxide. .								

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7030C	01/30/87	Th Oxide	NONE	G7006A, (8/40/60,+10), 24	8cts @ rpm		2@400	30@650inO2	LODM
	thermal oxide on 2"wafer; controlfor 7030B. .								
7030D	01/30/87	Th Oxide	B49	G7006A, (8/40/60,+10), 24	8cts @ rpm		2@400	30@650inO2	LODM
	Annealed after TEL deposition. .								
7035A	02/04/87	Th Oxide	NONE	G6307/7006A,	1/7cts @ rpm		2@400	30@650inO2	LODM
	Etched paddles - annealed 1/2 of wafer. .								
7035B	02/04/87	Th Oxide	NONE	G6307/7022,	1/7cts @ rpm		2@400	30@650inO2	LODM
	Etched paddles - annealed 1/2 of wafer. .								
7035C	02/04/87	Th Oxide	NONE	G6307/7020,	1/7cts @ rpm		2@400	30@650inO2	LODM
	Etched paddles - annealed 1/2 of wafer. .								
7035D	02/04/87	Si Wafer	NONE	G6307, (15/0/100,+10), 93	8cts @ rpm		2@400	30@650inO2	LODM
	Etched paddles - annealed 1/2 of wafer. .								
7036A	02/05/87	Si Wafer	B50-4	G6307/7006A,	1/7cts @ rpm		2@400	30@650inO2	LODM
	1"LODM; composite FES - 8/40/60 over 15/0/100. .								
7036B	02/05/87	Si Wafer	B50-4	G6307/7020,	1/7cts @ rpm		2@400	30@650inO2	LODM
	1"LODM; composite FES - 3/60/40 over 15/0/100. .								
7036C	02/05/87	Si Wafer	B50-4	G6307/7022,	1/7cts @ rpm		2@400	30@650inO2	LODM
	1"LODM; composite FES - 0/50/50 over 15/0/100. .								
7036D	02/05/87	Si Wafer	NONE	G6307/7006A,	1/7cts @ rpm		2@400	30@650inO2	LODM
	Etched paddles - annealed 1/2 of wafer. .								
7036E	02/05/87	Si Wafer	NONE	G7006A, (8/40/60,+10), 30	8cts @ rpm		2@400	30@650inO2	LODM
	Control for 7036A-D. .								
7037A	02/06/87	1000Å Ti	NONE	G6307/7006A,	1/7cts @ rpm		2@400	30@650inO2	LODM
	1000Å Ti over spin on oxide. .								
7037B	02/06/87	Oxide SpOn	NONE	G6307/7006A,	1/7cts @ rpm		2@400	30@650inO2	LODM
	Ti removed from spin on oxide. .								
7037C	02/06/87	500Å Ti	NONE	G6307/7006A,	1/7cts @ rpm		2@400	30@650inO2	LODM
	Ti thinned to about 500Å, thinner toward edge;spin on oxide. .								
7037D	02/06/87	1000Å Ti	NONE	G7006A, (8/40/60,+10), 31	8cts @ rpm		2@400	30@650inO2	LODM
	FES on spin on oxide control. .								
7037E	02/06/87	OxideORBTW	NONE	G6307/7006A,	1/7cts @ rpm		2@400	none	LODM
	1/4-Orbit TW with 209 oxide over nitride. .								
7037F	02/06/87	OxideORBTW	NONE	G6307/7006A,	1/7cts @ rpm		2@400	none	LODM
	1/4-Orbit TW with 209 oxide over nitride; HF dip. .								
7037G	02/06/87	OxideORBTW	NONE	G6307/7006A,	1/7cts @ rpm		2@400	none	LODM
	1/4-Orbit TW with 2 coats 209 oxide. .								
7038A	02/07/87	Orbit TW	NONE	G7006A, (8/40/60,+10), 32	8cts @ rpm		2@400	none	LODM
	1/4-Orbit TW with 2 coats 209 oxide. .								
7038B	02/07/87	Orbit TW	NONE	G7006A, (8/40/60,+10), 32	8cts @ rpm		2@400	none	LODM
	1/4-Orbit TW with 2 coats 209 oxide. .								
7040A	02/09/87	Orbit TW	NONE	G7006A, (8/40/60,+10), 34	8cts @ rpm		2@400	none	LODM
	1/4-Orbit TW with 2 coats 209 oxide. .								
7040B	02/09/87	Orbit TW	NONE	G7006A, (8/40/60,+10), 34	8cts @ rpm		2@400	none	LODM
	1/4-Orbit TW with 2 coats 209 oxide. .								
7042A	02/11/87	Orbit TW	NONE	G7006A, (8/40/60,+10), 36	8cts @ rpm		2@400	30@650inO2	LODM
	Thin Ti. .								

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7042B	02/11/87	Orbit TW	NONE	G7006A, (8/40/60,+10), 36	8cts @ rpm		2@400	30@650inO2	LODM
	Thin Ti. .								
7042C	02/11/87	Orbit TW	NONE	G7006A, (8/40/60,+10), 36	8cts @ rpm		2@400	30@650inO2	LODM
	Thin Ti. .								
7043A	02/12/87	OxideORBTW	NONE	G7006A, (8/40/60,+10), 37	8cts @ rpm		2@400	30@650inO2	LODM
	Thin Ti. .								
7043B	02/12/87	CMOS	NONE	G7006A, (8/40/60,+10), 37	8cts @ rpm		2@400	30@650inO2	LODM
	Thin Ti. .								
7044A	02/13/87	CMOS	B49	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	LODM
	Standard BEL; 1"LODM. .								
7044B	02/13/87	Oxide	B54-1	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	LODM
	250Å Ti/1500Å Pt;1"LODM. .								
7044C	02/13/87	Oxide	B54-2	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	LODM
	500Å Ti/750Å Pt; 1"LODM. .								
7044D	02/13/87	Oxide	B54-3	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	LODM
	500Å Ti/500Å Pt; 1"LODM. .								
7044E	02/13/87	Oxide	B54-1	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Int S
	1/4-4"wafer; paddle set; B54-1A etch. .								
7044F	02/13/87	Oxide	B54-2	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Int S
	1/4-4"wafer; paddle set; B54-2A etch. .								
7044G	02/13/87	Oxide	B54-3	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Int S
	1/4-4"wafer; paddle set. .								
7044H	02/13/87	Oxide	B54-1	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Int S
	1/4-4"wafer; paddle set; B54-1B etch. .								
7044I	02/13/87	Oxide	B54-2	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Int S
	1/4-4"wafer; paddle set; B54-2B etch. .								
7044J	02/13/87	Oxide	B54-3	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Int S
	1/4-4"wafer; paddle set. .								
7044K	02/13/87	CMOS	B54-3	G7006A, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Int S
	1/4-4"wafer; paddle set. .								
7048A	02/17/87	CMOS	B49	G7006A, (8/40/60,+10), 42	8cts @ rpm		2@400	inAr30@650	LODM
	Anneal in Argon. .								
7056A-1	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	Annealed immediately after coat/bake. .								
7056A-1	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	Same as 7056A-9 but H2NO3 dip after anneal. .								
7056A-2	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	Annealed ~72 hours after coat/bake. .								
7056A-3	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	R10 treatment then immediate anneal. .								
7056A-4	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	Immediate anneal then R10 treatment X2. .								
7056A-5	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	Simulate CMOS R10; immediate anneal. .								
7056A-6	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	Simulate CMOS with acetone/IPA; immediate anneal. .								

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7056A-7	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	Simulate CMOS with 130; immediate anneal. .								
7056A-8	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	Spin on PT; immediate anneal. .								
7056A-9	02/25/87	Oxide OrbTW	56-5	G7055, (8/40/60,+10), 1	8cts @ rpm		2@400	30@650inO2	LODM
	Annealed 72 hours after coat/bake but bake prior to anneal. .								
7059A	02/28/87	Oxide OrbTW	B50-4	G7047, (8/40/60,+10), 12	8cts @ rpm		2@400	30@650inO2	LODM
	New sol-gel test;suspect IPA(Alfa). .								
7059B	02/28/87	Oxide OrbTW	B50-4	G7055, (8/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	LODM
	Control for 7059A. .								
7069A	03/10/87	Oxide OrbTW	B57-2	G7055, (8/40/60,+10), 14	8cts @ rpm		2@400	30@650inO2	Fat1
	Imm. anneal. .								
7069B	03/10/87	Oxide OrbTW	B57-3	G7055, (8/40/60,+10), 14	8cts @ rpm		2@400	30@650inO2	Fat1
	Imm. anneal. .								
7069C	03/10/87	Oxide OrbTW	B57-4	G7055, (8/40/60,+10), 14	8cts @ rpm		2@400	30@650inO2	Fat1
	Imm. anneal. .								
7069D	03/10/87	Oxide OrbTW	B57-5	G7055, (8/40/60,+10), 14	8cts @ rpm		2@400	30@650inO2	Fat1
	Imm. anneal. .								
7075A	03/16/87	Oxide OrbTW	B60-1	G7055, (8/40/60,+10), 20	8cts @ rpm		2@400	30@650inO2	Fat1
	Imm. anneal. .								
7075B	03/16/87	Oxide OrbTW	B60-2	G7055, (8/40/60,+10), 20	8cts @ rpm		2@400	30@650inO2	Fat1
	Imm. anneal. .								
7075C	03/16/87	ASM32	B60-2	G7047, (8/40/60,+10), 28	8cts @ rpm		2@400	none	Fat1
	ASM aligner test. .								
7075D	03/16/87	ASM33	B60-2	G7047, (8/40/60,+10), 28	8cts @ rpm		2@400	none	Fat1
	ASM aligner test. .								
7075E	03/16/87	ASM35	B60-2	G7047, (8/40/60,+10), 28	8cts @ rpm		2@400	30@650inO2	Fat1
	ASM aligner test. .								
7076A	03/17/87	?	B62-1	G7072, (3/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat1
	3/40/60,+10;imm.anneal. .								
7076B	03/17/87	?	B62-2	G7022, (0/50/50,+10), 54	8cts @ rpm		2@400	30@650inO2	Fat1
	0/50/50,+10;imm.anneal. .								
7076C	03/17/87	?	B62-4	G7068, (15/0/100,+10), 8	8cts @ rpm		2@400	30@650inO2	Fat1
	15/0/100,+10;imm.anneal. .								
7077A	03/18/87	?	B61-2	G7022, (0/50/50,+10), 55	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;0/50/50. .								
7077B	03/16/87	?	B61-2	G7072, (3/40/60,+10), 5	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;3/40/60. .								
7077C	03/18/87	?	B61-2	G7020, (3/60/40,+10), 57	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;3/60/40. .								
7077D	03/18/87	?	B61-2	G7047, (8/40/60,+10), 30	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;8/40/60. .								
7077E	03/18/87	Si Wafer	NONE	G7068/7047,	1/7cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7077F	03/18/87	Th Oxide	NONE	G7068/7047,	1/7cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								

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7082A	03/23/87	Orbit TW	B58-4	G7055, (8/40/60,+10), 27	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7082B	03/23/87	Orbit TW	B64-1	G7055, (8/40/60,+10), 27	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7082C	03/23/87	CMOS	B56-3	G7055, (8/40/60,+10), 27	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7082D	03/23/87	Orbit TW	B64-2	G7055, (8/40/60,+10), 27	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7082E	03/23/87	Orbit TW	B64-3	G7055, (8/40/60,+10), 27	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7082F	03/23/87	Orbit TW	B64-4	G7055, (8/40/60,+10), 27	8cts @ rpm		2@400	30@650inO2	LODM
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7085B	03/26/87	Th Oxide	B65-2	G7047, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Fat1
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7085C	03/26/87	Th Oxide	B65-3	G7047, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Fat1
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7085D	03/26/87	Th Oxide	B65-4	G7047, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Fat1
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7085E	03/26/87	Th Oxide	B65-5	G7047, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	Fat1
	Diana's 1st;composite test, 15/0/100 under 8/40/60. .								
7086A	03/27/87	Th Oxide	B65-1	GGB7085, (3/40/60,+10), 18/64	8cts @ rpm		2@400	30@650inO2	Fat1
	GB7085 is 80/20 blend of G7022 and G7068 giving a 3/40/60,+10. .								
7089A	03/30/87	Th Oxide	B63-1	G7055, (8/40/60,+10), 34	8cts @ rpm		2@400	30@650inO2	Fat1
	6000Å oxide/TiO2/Pt; no Ti in field. .								
7089B	03/30/87	Th Oxide	B66-1	G7055, (8/40/60,+10), 34	8cts @ rpm		2@400	30@650inO2	LODM
	Sectioned for 1" LODM's; TEL barrier study; 7089B-1 thru 8. .								
7093A	04/03/87	ASM F>B	B66-1	G7047, (8/40/60,+10), 46	8cts @ rpm		2@400	30@650inO2	LODM
	Sectioned for 1" LODM's; TEL barrier study; 7089B-1 thru 8. .								
7093B	04/03/87	ASM F>B	B66-1	G7047, (8/40/60,+10), 46	8cts @ rpm		2@400	30@650inO2	LODM
	Sectioned for 1" LODM's; TEL barrier study; 7089B-1 thru 8. .								
7094A	04/04/87	Th Oxide	B61-1	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; standard anneal. .								
7094B	04/04/87	Th Oxide	B61-3	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; 48 hrs before std. anneal. .								
7094C	04/04/87	Th Oxide	B61-4	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; 2in/min ramp-in/out,30"@650°anneal. .								
7094D	04/04/87	Th Oxide	B61-5	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; fast ramp-in/out,30"@650°anneal. .								
7094E	04/04/87	Th Oxide	B62-5	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; 48 hrs before std. anneal. .								
7094F	04/04/87	Th Oxide	B63-2	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; standard anneal. .								
7094G	04/04/87	Th Oxide	B63-3	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; 48 hrs before std. anneal. .								
7094H	04/04/87	Th Oxide	B63-4	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; 2in/min ramp-in/out,30"@650°anneal. .								

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7094I	04/04/87	Th Oxide	B63-5	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; fast ramp-in/out,30"@650°anneal. .								
7094J	04/04/87	Th Oxide	B66-2	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; 48 hrs before std. anneal. .								
7094K	04/04/87	Th Oxide	B66-3	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study; 48 hrs before std. anneal. .								
7094L	04/04/87	Th Oxide	B67-1	G7047, (8/40/60,+10), 47	8cts @ rpm		2@400	30@650inO2	Fat1
	Scratch protection study;FES lifting in field at dep. ct.8. .								
7096A	04/06/87	Th Oxide	B50-4	G7090B, (8/40/60,+30°), 6	5cts @ rpm		2@400	30@650inO2	Fat1
	2000rpm spin, DEKTAK; crazing by 4th coat; stopped coating. .								
7096B	04/06/87	Th Oxide	B50-4	G709OB, (8/40/60,+30°), 6	5cts @ rpm		2@400	30@650inO2	Fat1
	4000rpm spin, DEKTAK. .								
7096C	04/06/87	Th Oxide	B66-4	G7090A, (8/40/60,+0), 6	8cts @ rpm		2@400	30@650inO2	LODM
	Excess Pb study. .								
7096D	04/06/87	Th Oxide	B66-4	G7091, (8/40/60,+30), 5	8cts @ rpm		2@400	30@650inO2	LODM
	Excess Pb study. .								
7096E	04/06/87	Th Oxide	B66-4	G7092, (6/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	LODM
	New composition. .								
7096F	04/06/87	Th Oxide	B66-4	G7047, (8/40/60,+10), 49	8cts @ rpm		2@400	MufFur650	LODM
	Fast ramp study. .								
7096G	04/06/87	Th Oxide	B66-4	G7047, (8/40/60,+10), 49	8cts @ rpm		2@400	2"/-650°	LODM
	Slow ramp study. .								
7096H	04/06/87	Th Oxide	B66-4	G7072, (3/40/60,+10), 24	8cts @ rpm		2@400	30@650inO2	LODM
	Control for 7096I. .								
7096I	04/06/87	Th Oxide	B66-4	GB7085, (3/40/60,+10), 28/74	8cts @ rpm		2@400	30@650inO2	LODM
	Blended Gel. .								
7096J	04/06/87	Th Oxide	B66-4	G7090B, (8/40/60,+30°), 6	4cts @ rpm		2@400	30@650inO2	LODM
	2X std. sol-gel concentration; stopped at 4th coat; annealed. .								
7097A	04/07/87	Th Oxide	B66-4	G7090B, (8/40/60,+30°), 7	4cts @ rpm		2@400	30@650inO2	LODM
	2X std. sol-gel concentration; spin 4 coats at 4000 rpm. .								
7097B	04/07/87	Orbit TW	B70-3	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	TDO1
	Pre 512 process tune-up. .								
7097C	04/07/87	Orbit TW	B71-3	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	TDO1
	Pre 512 process tune-up. .								
7097D	04/07/87	CMOS	B71-4	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	TDO1
	Pre 512 process tune-up. .								
7097E	04/07/87	Orbit TW	B70-1	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	TDO1
	Pre 512 process tune-up. .								
7097F	04/07/87	CMOS	B71-5	G7047, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	TDO1
	Pre 512 process tune-up. .								
7098A	04/08/87	Th Oxide	B66-5	G7047, (8/40/60,+10), 51	24cts @ rpm		2@400	30@650inO2	TDO1
	24 coats (3x8), anneal after each 8 cts. For Dr.McInerney.. .								
7098B	04/08/87	Th Oxide	B66-5	G7047, (8/40/60,+10), 51	24cts @ rpm		2@400	30@650inO2	TDO1
	24 coats (3x8), anneal after each 8 cts. For Dr.Land.. .								
7098C	04/08/87	Th Oxide	B66-5	G7020, (3/60/40,+10), 78	24cts @ rpm		2@400	30@650inO2	TDO1
	24 coats (3x8), anneal after each 8 cts. For Dr.McInerney.. .								

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7098D	04/08/87	Th Oxide	B66-5	G7020, (3/60/40,+10), 78	24cts @ rpm		2@400	30@650inO2	TDO1
	24 coats (3x8), anneal after each 8 cts. For Dr.Land.. .								
7098E	04/08/87	TW ECD512	B73-2	G7047, (8/40/60,+10), 51	8cts @ rpm		2@400	30@650inO2	512
	ECD512 test wafer. .								
7098F	04/08/87	TW ECD512	B73-3	G7047, (8/40/60,+10), 51	8cts @ rpm		2@400	30@650inO2	512
	ECD512 test wafer. .								
7098G	04/08/87	Th Oxide	B66-5	G7047, (8/40/60,+10), 51	32cts @ rpm		2@400	30@650inO2	512
	Multiples of 8 coats, anneal after each 8 cts. .								
7099A	04/09/87	Nitride	B66-5	G7047, (8/40/60,+10), 52	8cts @ rpm		2@400	30@650inO2	512
	FES over single layer spin-on Ti900(oxidized @ 650 for 30 min). .								
7100A	04/10/87	Nitride	B66-5	G7047, (8/40/60,+10), 53	8cts @ rpm		2@400	30@650inO2	512
	FES over two layers spin-on Ti900(oxidized @ 650 for 30 min). .								
7100B	04/10/87	Nitride	B66-5	G7047, (8/40/60,+10), 53	8cts @ rpm		2@400	30@650inO2	512
	FES over two layers spin-on Ti900(oxidized @ 750 for 30 min). .								
7104A	04/14/87	CMOS	B75-1	G7055, (8/40/60,+10), 49	8cts @ rpm		2@400	30@650inO2	TDO1
	FES over two layers spin-on Ti900(oxidized @ 750 for 30 min). .								
7104B	04/14/87	CMOS	B75-2	G7055, (8/40/60,+10), 49	8cts @ rpm		2@400	30@650inO2	TDO1
	FES over two layers spin-on Ti900(oxidized @ 750 for 30 min). .								
7104C	04/14/87	TW ECD512	B74-2	G7055, (8/40/60,+10), 49	8cts @ rpm		2@400	30@650inO2	512
	ECD512 test wafer. .								
7104D	04/14/87	TW ECD512	B74-3	G7055, (8/40/60,+10), 49	8cts @ rpm		2@400	30@650inO2	512
	ECD512 test wafer. .								
7105A	04/15/87	TW ECD512	B76-1	G7055, (8/40/60,+10), 50	8cts @ rpm		2@400	30@590inO2	512
	ECD512 test wafer. .								
7105B	04/15/87	TW ECD512	B76-2	G7055, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	512
	ECD512 test wafer. .								
7105C	04/15/87	ECD512A	B76-3	G7055, (8/40/60,+10), 50	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A. .								
7105D	04/15/87	ECD512A	B76-4	G7055, (8/40/60,+10), 50	8cts @ rpm		2@400	30@590inO2	512
	CMOS ECD512A. .								
7106A	04/16/87	Th Oxide	B56-3	G7072, (3/40/60,+10), 34	8cts @ rpm		2@400	30@650inO2	LODM
	Control for 7106 film series. .								
7106B	04/16/87	Th Oxide	B56-3	GB7085, (3/40/60,+10), 21	8cts @ rpm		2@400	30@650inO2	LODM
	GB7085 is 80/20 blend of G7022 and G7068 giving a 3/40/60,+10. .								
7106C	04/16/87	Th Oxide	B56-3	GB7106A, (5.5/40/60,+5), <1	8cts @ rpm		2@400	30@650inO2	LODM
	GB7106A is 50/50 blend of G7072 & G7090A; 5.5/40/60,+5. .								
7106D	04/16/87	Th Oxide	B56-3	GB7106B, (5.5/40/60,+10), <1	8cts @ rpm		2@400	30@650inO2	LODM
	GB7106B is 50/50 blend of G7072 & G7055; 5.5/40/60,+10. .								
7106E	04/16/87	Th Oxide	B56-3	GB7106C, (5.5/40/60,+15), <1	8cts @ rpm		2@400	30@650inO2	LODM
	GB7106C is 1/2:1/6:1/3 blend of G7072:7090A:7091;5.5/40/60,+15. .								
7106F	04/16/87	Th Oxide	B56-3	GB7106D, (8/40/60,+5), <1	8cts @ rpm		2@400	30@650inO2	LODM
	GB7106D is 5/6:1/6 blend of G7090A & 7091; 8/40/60,+5. .								
7106G	04/16/87	Th Oxide	B56-3	GB7106E, (8/40/60,+15), <1	8cts @ rpm		2@400	30@650inO2	LODM
	GB7106E is 50:50 blend of G7090A & 7091; 8/40/60,+15. .								
7106H	04/16/87	Th Oxide	B56-3	G7055, (8/40/60,+10), 51	8cts @ rpm		2@400	30@650inO2	LODM
	Control for 7106 film series. .								

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7114A	04/24/87	Nit+TiO2	T-1	G7110, (8/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat1
	550Å TiO2 under BEL study; 500Å Ti/1000Å Pt. Accuglass 305;3000rpm;2/ramp out @465°C/2 in O2;bottom half.								
7114B	04/24/87	Nit+TiO2	T-2	G7110, (8/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat1
	750Å TiO2 under BEL study; 500Å Ti/1000Å Pt. Accuglass 305;3000rpm;2/ramp out @465°C/2 in O2;bottom half.								
7114C	04/24/87	Nit+TiO2	T-3	G7110, (8/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat1
	1050Å TiO2 under BEL study; 500Å Ti/1000Å Pt. Accuglass 305;3000rpm;2/ramp out @465°C/2 in O2;bottom half.								
7114D	04/24/87	Nitride	B78-4	G7110, (8/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat1
	Nitride under 850Å Ti/1000Å Pt. .								
7114E	04/24/87	Th Oxide	B78-2	G7110, (8/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat1
	Oxide under 850Å Ti/1000Å Pt. .								
7114F	04/24/87	Th Oxide	B68-3	G7110, (8/40/60,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat1
	Spin-on oxide/interlevel dielectric study. .								
7114G	04/24/87	Th Oxide	B68-4	G7110, (8/40/60,+10), 4	7cts @ rpm		2@400	30@650inO2	Fat1
	Spin-on oxide/interlevel dielectric study;FES lifting @ 7th ct. .								
7114H	04/24/87	Th Oxide	B68-5	G7110, (8/40/60,+10), 4	5cts @ rpm		2@400	30@650inO2	Fat1
	Spin-on oxide/interlevel dielectric study;FES lifting @ 5th ct. .								
7117A	04/27/87	TD01 CMOS	B77-5	G7110, (8/40/60,+10), 7	8cts @ rpm		2@400	30@650inO2	TDO1
	TD01 CMOS with nitride removed pre-BEL. .								
7117B	04/27/87	ECD512A	B78-1	G7110, (8/40/60,+10), 7	8cts @ rpm		2@400	30@650inO2	512
	TiO2 pad in place prior to BEL; 1000Å Ti oxidized. .								
7120A	04/30/87	Th Oxide	B67-2	G7110, (8/40/60,+10), 10	8cts @ rpm		2@400	30@650inO2	Fat1
	Spin-on oxide/interlevel dielectric study;FES lifting @ 8th ct. .								
7120B	04/30/87	Th Oxide	B67-3	G7110, (8/40/60,+10), 10	8cts @ rpm		2@400	30@650inO2	Fat1
	Spin-on oxide/interlevel dielectric study. .								
7120C	04/30/87	Th Oxide	B67-4	G7110, (8/40/60,+10), 10	8cts @ rpm		2@400	30@650inO2	Fat1
	Spin-on oxide/interlevel dielectric study. .								
7120D	04/30/87	Th Oxide	B67-5	G7110, (8/40/60,+10), 10	8cts @ rpm		2@400	30@650inO2	Fat1
	Spin-on oxide/interlevel dielectric study. .								
7121A	05/01/87	1000Å TiO2	B79-1	G7110/7072,	1/6/1cts @ rpm		2@400	30@650inO2	Fat1
	Buffer layer study;1x8/40/60,+10:6x3/40/60,+10:1x8/40/60,+10. .								
7121B	05/01/87	1000Å TiO2	B79-2	G7068/7022,	1/6/1cts @ rpm		2@400	30@650inO2	Fat1
	Buffer layer study; blistered after sinter. .								
7121C	05/01/87	1000Å TiO2	B79-3	G7068/7020,	1/6/1cts @ rpm		2@400	30@650inO2	Fat1
	Buffer layer study; blistered after sinter. .								
7125A	05/05/87	ASM833	B79-3	G7110, (8/40/60,+10), 15	8cts @ rpm		2@400	No Anneal	Fat1
	ASM aligner test. .								
7125B	05/05/87	ASM832	B79-3	G7110, (8/40/60,+10), 15	8cts @ rpm		2@400	No Anneal	Fat1
	ASM aligner test. .								
7125C	05/05/87	Nitride	B80-1	G7022, (0/50/50,+10), 103	4cts @ rpm		2@400	30@650inO2	Fat1
	1/2 Std. FES thickness. .								
7125D	05/05/87	Nitride	B80-3	G7072, (3/40/60,+10), 53	4cts @ rpm		2@400	30@650inO2	Fat1
	1/2 Std. FES thickness. .								
7125E	05/05/87	Nitride	B80-4	G7110, (8/40/60,+10), 15	4cts @ rpm		2@400	30@650inO2	Fat1
	1/2 Std. FES thickness. .								
7125F	05/05/87	ECD512A	B81-1	G7110, (8/40/60,+10), 15	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A. .								

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7131A	05/11/87	Th Ox,TiO2	B79-4	G7020, (3/60/40,+10), 111	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue test of 3/60/40,+10. .								
7132A	05/12/87	Th Oxide	B7?-?	G7110, (8/40/60,+10), 22	8cts @ rpm		2@400	30@650inO2	LODM
	Ion Gun Etch Studies. .								
7132B	05/12/87	Nit(35-)	NA	G7110, (8/40/60<=10), 22	4cts @ rpm		2@400	30@650inO2	NA
	Spin-on TiO2 over nitride study. .								
7135A	05/15/87	Th Oxide	B56-4	G7110, (8/40/60,+10), 25	8cts @ rpm		2@400	30@650inO2	LODM
	Ion Gun Etch Studies. .								
7135B	05/15/87	ECD512A	B56-4	G7110, (8/40/60,+10), 25	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A. .								
7135C	05/15/87	ECD512A	B56-4	G7110, (8/40/60,+10), 25	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A;alloy Al for 10min@400°C. .								
7139A	05/19/87	ECD512A	B56-4	G7022, (0/50/50,+10), 117	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A. .								
7142A	05/22/87	Nitride	B56-4	G7141, (0/50/50,+10), 1	8cts @ rpm		2@400	30@650inO2	NA
	Test new 0/50/50,+10. .								
7142B	05/22/87	Nitride	B56-4	G7141, (0/50/50,+10), 1	8cts @ rpm		2@400	30@650inO2	NA
	Test new 0/50/50,+10. .								
7142C	05/22/87	Si Wafer	B56-4	G7068/7141,	1/7cts @ rpm		2@400	30@650inO2	NA
	For UNM optical measurements. .								
7148A	05/28/87	ECD512A	B86	G7110, (8/40/60,+10), 38	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 8/40/60,+10. .								
7148B	05/28/87	ECD512A	B86	G7141, (0/50/50,+10), 7	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10. .								
7148C	05/28/87	Th Oxide	NA	G6307/7141,	1/7cts @ rpm		2@400	30@650inO2	NA
	Buffer layer on SiO2;older 15/0/100 gel. .								
7148D	05/28/87	Th Oxide	NA	G7068/7141,	1/7cts @ rpm		2@400	30@650inO2	NA
	Buffer layer on SiO2;newer 15/0/100 gel. .								
7148E	05/28/87	Si Wafer	NA	G6307/7141,	1/7cts @ rpm		2@400	30@650inO2	NA
	Buffer layer on Si;older 15/0/100 gel. .								
7148F	05/28/87	Si Wafer	NA	G7068/7141,	1/7cts @ rpm		2@400	30@650inO2	NA
	Buffer layer on Si;newer 15/0/100 gel. .								
7152A	06/01/87	Th Ox,TiO2	B85-2	G7110/7141,	1/6/1cts @ rpm		2@400	30@650inO2	Fat1
	Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 380°c.								
7152B	06/01/87	Th Ox,TiO2	B85-3	G7092, (6/50/50,+10), 60	8cts @ rpm		2@400	30@650inO2	Fat1
	Buffer layers;8/40/60 on 6x0/50/50 on 8/40/60. Metal alloyed 10min @ 380°c.								
7152C	06/01/87	Th Ox,TiO2	B85-4	G7141, (0/50/50,+10), 11	6cts @ rpm		2@400	30@650inO2	Fat1
	Film thinness study;etch top half before anneal. Metal alloyed 10min @ 380°C.								
7152D	06/01/87	Th Ox,TiO2	B85-5	G7110, (8/40/60,+10), 42	6cts @ rpm		2@400	30@650inO2	Fat1
	Film thinness study;etch before anneal. Metal alloyed 10min @ 380°C.								
7155A	06/04/87	Th Ox,TiO2	B79-5	G7153, (0/50/50,+0), 2	8cts @ rpm		2@400	30@650inO2	Fat1
	New composition;0/50/50,+0;anneal bottom half at 650,. anneal top half at 750°C;alloy metal 10min at 400°C.								
7155B	06/04/87	Th Ox,TiO2	B82-1	G7154, (1/45/55,+10), 1	8cts @ rpm		2@400	30@650inO2	Fat1
	New Composition;1/45/55,+10. Metal alloyed 10min @ 380°C.								
7155C	06/04/87	Th Ox,TiO2	B82-2	G7155, (0/40/60,+10), <1	8cts @ rpm		2@400	30@650inO2	Fat1
	New composition;0/40/60,+10. Metal alloyed 10min @ 380°C.								

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7156A	06/05/87	ECD512A#7	B85-1	G7141, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10. .								
7156B	06/05/87	ECD512A#9	B86-?	G7141, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10. .								
7160A	06/09/87	ECD512A#13	B86-?	G7141, (0/50/50,+10), 19	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;metal annealed 10min @ 400°C. .								
7162A	06/11/87	ECD512A#3	B91-?	G7141, (0/50/50,+10), 21	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;10min @ 400°C metal anneal. .								
7162B	06/11/87	ECD512A#16	B91-?	G7141, (0/50/50,+10), 21	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10. .								
7162C	06/11/87	ECD512A#20	B91-?	G7141, (0/50/50,+10), 21	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;10min @ 400°C metal anneal. .								
7162D	06/11/87	ECD512A#22	B91-?	G7141, (0/50/50,+10), 21	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;metal annealed 10min @ 400°C. .								
7166A	06/15/87	ECD512A#16	B91-?	G7141, (0/50/50,+10), 25	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;FES rework of 7162B. .								
7166B	06/15/87	Th Ox,TiO2	B82-3	G7141, (0/50/50,+10), 25	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue test of 0/50/50,+10. .								
7166C	06/15/87	Th Ox,TiO2	B82-4	G7141, (0/50/50,+10), 25	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue test of 0/50/50,+10. .								
7166D	06/15/87	Th Ox,TiO2	B82-5	G7153, (0/50/50,+0), 13	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue test of 0/50/50,+0. .								
7167A	06/16/87	TDO1	B92-?	G7141, (0/50/50,+10), 26	8cts @ rpm		2@400	30@650inO2	TDO1
	Annealing test;TiN composition. .								
7167B	06/16/87	TDO1	B92-?	G7141, (0/50/50,+10), 26	8cts @ rpm		2@400	30@650inO2	TDO1
	Annealing test;TiN composition. .								
7167C	06/16/87	TDO1	B92-?	G7141, (0/50/50,+10), 26	8cts @ rpm		2@400	30@650inO2	TDO1
	Annealing test;TiN composition. .								
7167D	06/16/87	TDO1	B92-?	G7141, (0/50/50,+10), 26	8cts @ rpm		2@400	30@650inO2	TDO1
	Annealing test;TiN composition. .								
7168A	06/17/87	Th Ox,TiO2	B68-1	G7141, (0/50/50,+10), 27	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue pattern for ILD study;FES peeling at 8th coat. .								
7168B	06/17/87	Th Ox,TiO2	B68-2	G7141, (0/50/50,+10), 27	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue pattern for ILD study;wafer shattered on HP at 1st ct. .								
7168C	06/17/87	Th Ox,TiO2	B69-1	G7141, (0/50/50,+10), 27	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue pattern for ILD study. .								
7168D	06/17/87	Th Ox,TiO2	B69-2	G7141, (0/50/50,+10), 27	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue pattern for ILD study;FES peeling at 8th coat. .								
7168E	06/17/87	Th Ox,TiO2	B69-3	G7141, (0/50/50,+10), 27	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue pattern for ILD study. .								
7168F	06/17/87	Th Ox,TiO2	B69-4	G7141, (0/50/50,+10), 27	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue pattern for ILD study. .								
7168G	06/17/87	Th Ox,TiO2	B69-5	G7141, (0/50/50,+10), 27	8cts @ rpm		2@400	30@650inO2	Fat1
	Fatigue pattern for ILD study. .								
7173A	06/22/87	Th Ox,TiO2	B87-1	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								

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7173B	06/22/87	Th Ox,TiO2	B87-2	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7173C	06/22/87	Th Ox,TiO2	B87-3	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7173D	06/22/87	Th Ox,TiO2	B87-4	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7173E	06/22/87	Th Ox,TiO2	B87-5	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7173F	06/22/87	Th Ox,TiO2	B88-1	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7173G	06/22/87	Th Ox,TiO2	B88-2	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7173H	06/22/87	Th Ox,TiO2	B88-3	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	. .								
7173I	06/22/87	Th Ox,TiO2	B88-4	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7173J	06/22/87	Th Ox,TiO2	B88-5	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	Fat2
	. .								
7173K	06/22/87	Th Ox,TiO2	B78-3	G7170, (0/50/50,+10), 3	8cts @ rpm		2@400	30@650inO2	NA
	Etch test. .								
7175A	06/24/87	ECD512A#5	96or97	G7170, (0/50/50,+10), 5	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7175B	06/24/87	ECD512A#10	96or97	G7170, (0/50/50,+10), 5	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7175C	06/24/87	ECD512A#24	96or97	G7170, (0/50/50,+10), 5	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. Wafer broken during processing, 1/2+ remaining.								
7175D	06/24/87	Th Ox,TiO2	B89-1	G7153, (0/50/50,+0), 22	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7175E	06/24/87	Th Ox,TiO2	B89-2	G7153, (0/50/50,+0), 22	8cts @ rpm		2@400	30@650inO2	Fat2
	. .								
7175F	06/24/87	Th Ox,TiO2	B89-3	G7153, (0/50/50,+0), 22	8cts @ rpm		2@400	30@650inO2	Fat2
	Shattered during 1st coat bake. .								
7175G	06/24/87	Th Ox,TiO2	B89-4	G7153, (0/50/50,+0), 22	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7175H	06/24/87	Th Ox,TiO2	B90-5	G7170, (0/50/50,+10), 5	10*cts @ rpm		2@400	30@650inO2	LODM
	Accuglass Ti-900 as 1st and 10th coats;3000rpm,std FES bake. Alternate electrode screening;occasional wide spaced cracks.								
7177A	06/26/87	ECD512A#12	96or97	G7170, (0/50/50,+10), 7	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10. .								
7183A	07/02/87	Orb512TW	?	G7170, (0/50/50,+10), 13	8cts @ rpm		2@400	30@650inO2	512
	ILD study. .								
7183B	07/02/87	Orb512TW	?	G7170, (0/50/50,+10), 13	8cts @ rpm		2@400	30@650inO2	512
	ILD study. .								
7183C	07/02/87	Orb512TW	?	G7170, (0/50/50,+10), 13	8cts @ rpm		2@400	30@650inO2	512
	ILD study. .								
7183D	07/02/87	Orb512TW	?	G7170, (0/50/50,+10), 13	8cts @ rpm		2@400	30@650inO2	512
	ILD study. .								

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7187A	07/06/87	04m129#6	?	G7170, (0/50/50,+10), 17	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7187B	07/06/87	04m129#14	?	G7170, (0/50/50,+10), 17	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7187C	07/06/87	04m129#15	?	G7170, (0/50/50,+10), 17	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7187D	07/06/87	04m129#17	?	G7170, (0/50/50,+10), 17	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7187E	07/06/87	04m129#21	?	G7170, (0/50/50,+10), 17	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7190A	07/09/87	06m061#1	B100-1	G7170, (0/50/50,+10), 20	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. Reworked from BEL.								
7190B	07/09/87	06m061#9	B100-2	G7170, (0/50/50,+10), 20	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. Reworked from BEL.								
7190C	07/09/87	?	B53-2	G7170, (0/50/50,+10), 20	8cts @ rpm		2@400	30@650inO2	512
	FES etch studies, 0/50/50,+10. .								
7203A	07/22/87	Unifilm#1	Uf#1	G7194, (0/50/50,+10), 9	8cts @ rpm		2@400	30@650inO2	Fat2
	1st BEL from Unifilm sputterer. .								
7204A	07/23/87	Th Oxide	NA	G7170, (0/50/50,+10), 34	8cts @ rpm		2@400	NA	NA
	Semi-Auto sol-gel dispense with EFD system. .								
7204B	07/23/87	Th Ox,TiO2	102-1	G7194, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	NA
	ILD study. .								
7204C	07/23/87	Th Ox,TiO2	102-2	G7194, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	NA
	ILD study. .								
7204D	07/23/87	Th Ox,TiO2	102-3	G7194, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	NA
	ILD study. .								
7204E	07/23/87	Th Ox,TiO2	102-4	G7194, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	NA
	ILD study. .								
7204F	07/23/87	Th Ox,TiO2	102-5	G7194, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	NA
	ILD study. .								
7205A	07/24/87	06m061#2	BM103	G7194, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.								
7205B	07/24/87	06m061#5	BM103	G7194, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.								
7205C	07/24/87	06m061#11	BM103	G7194, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.								
7205D	07/24/87	06m061#20	BM103	G7194, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.								
7205E	07/24/87	06m061#25	BM103	G7194, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. 1st sinter reached 610°C only; 2nd sinter, 30min@650°C.								
7209A	07/28/87	?	?	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7209B	07/28/87	?	?	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7209C	07/28/87	?	?	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								

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7209D	07/28/87	?	?	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7209E	07/28/87	Th Ox,TiO2	104-1	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7209F	07/28/87	Th Ox,TiO2	104-2	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7209G	07/28/87	Th Ox,TiO2	104-3	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7209H	07/28/87	Th Ox,TiO2	104-4	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7209I	07/28/87	Th Ox,TiO2	104-5	G7194, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	ILD study. .								
7211A	07/30/87	06m061#3t	104-5	G7194, (0/50/50,+10), 16	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. Top half of wafer.								
7211B	07/30/87	06m061#7	104-5	G7194, (0/50/50,+10), 16	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7211C	07/30/87	06m061#18	104-5	G7194, (0/50/50,+10), 16	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7211D	07/30/87	06m061#22	104-5	G7194, (0/50/50,+10), 16	8cts @ rpm		2@400	30@650inO2	512
	CMOS ECD512A with 0/50/50,+10;alloy metal 10min at 400°C. .								
7211E	07/30/87	06m061#3b	Gone	G7194, (0/50/50,+10), 16	8cts @ rpm		2@400	30@650inO2	512
	Failure analysis;cracking/furrowing around TiO2. Bottom half of wafer.								
7212A	07/31/87	06m079#2	NA	G7194, (0/50/50,+10), 17	8cts @ rpm		2@375	30@650inO2	512
	#1;1400Å Ti(normal Ti,1000Å). .								
7212B	07/31/87	06m079#21	NA	G7194, (0/50/50,+10), 17	8cts @ rpm		2@375	30@650inO2	512
	#2;1000Å Ti(normal Ti,1000Å). .								
7212C	07/31/87	06m079#11	NA	G7194, (0/50/50,+10), 17	8cts @ rpm		2@375	30@650inO2	512
	#4;500Å Ti(normal Ti,1000Å). .								
7212D	07/31/87	08m079#19	NA	G7194, (0/50/50,+10), 17	8cts @ rpm		2@425	30@650inO2	512
	#3;1000Å Ti(normal Ti,1000Å). .								
7212E	07/31/87	06m079#16	NA	G7194, (0/50/50,+10), 17	8cts @ rpm		2@425	30@650inO2	512
	#5;500Å Ti(normal Ti,1000Å). .								
7218A	08/06/87	1x1/16quartz	NA	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	NA
	UNM optical studies. .								
7218B	08/06/87	1x1/16quartz	NA	G7068/7194,	1/7cts @ rpm		2@400	30@650inO2	NA
	UNM optical studies. .								
7218C	08/06/87	1x1/16quartz	NA	G7068, (15/0/100,+10), 150	8cts @ rpm		2@400	30@650inO2	NA
	UNM optical studies. .								
7218D	08/06/87	Th Ox,TiO2	?	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
	85HB5;TiP-7;#01. .								
7218E	08/06/87	Th Ox,TiO2	?	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
	P42;85HB5;Ti-10;#02. .								
7218F	08/06/87	Th Ox,TiO2	?	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
	P32;84HB9;Ti-8;#03. .								
7218G	08/06/87	Th Ox,TiO2	?	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
	83HB9;TiP-5;#04. .								

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7218H	08/06/87	Th Ox,TiO2 P22;85HB10;Ti-6;#05. .	?	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
7218I	08/06/87	Th Ox,TiO2 P21;84HB10;Ti-5;#06. .	?	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
7218J	08/06/87	Th Ox,TiO2 P41;83B4;Ti-9;#07. .	?	G7194, (0/50/50,+10), 24	8cts @ rpm		2@400	30@650inO2	Fat2
7222A	08/10/87	06m061 Titanium over BEL. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	512
7222B	08/10/87	06m061#13 Titanium over BEL. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	512
7222C	08/10/87	06m061#14 Titanium over BEL. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	512
7222D	08/10/87	06m061#17 Titanium over BEL. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	512
7222E	08/10/87	06m061#1? Titanium over BEL. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	512
7222F	08/10/87	06m061#4 Standard BEL. .	STD BEL	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	512
7222G	08/10/87	06m061#10 Standard BEL. .	STD BEL	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	512
7222H	08/10/87	06m061#8 Standard BEL. .	STD BEL	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	512
7222I	08/10/87	Th Ox,TiO2 Titanium over BEL;top half cleared. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	Fat2
7222J	08/10/87	Th Ox,TiO2 Titanium over BEL. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	Fat2
7222K	08/10/87	Th Ox,TiO2 Titanium over BEL. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	Fat2
7222L	08/10/87	Th Ox,TiO2 Titanium over BEL. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	Fat2
7222M	08/10/87	Th Ox,TiO2 Titanium over BEL. .	TI/PT/TI	G7194, (0/50/50,+10), 28	8cts @ rpm		2@400	30@650inO2	Fat2
7234A	08/22/87	Th Ox,TiO2 Std.BEL; FES coated/baked/sintered in new facility. G7225 first sol-gel made in new facility on new apparatus.	11-1	G7225, (0/50/50,+10), 9	8cts @ rpm		2@400	30@650inO2	Fat2
7234B	08/22/87	Th Ox,TiO2 Std.BEL; FES coated/baked/sintered in new facility. G7225 first sol-gel made in new facility on new apparatus.	11-2	G7225, (0/50/50,+10), 9	8cts @ rpm		2@400	30@650inO2	Fat2
7234C	08/22/87	Th Ox,TiO2 Std.BEL; FES coated/baked/sintered in new facility. G7225 first sol-gel made in new facility on new apparatus.	11-3	G7225, (0/50/50,+10), 9	8cts @ rpm		2@400	30@650inO2	Fat2
7234D	08/22/87	Th Ox,TiO2 Std.BEL; FES coated/baked/sintered in new facility. G7225 first sol-gel made in new facility on new apparatus.	11-4	G7225, (0/50/50,+10), 9	8cts @ rpm		2@400	30@650inO2	Fat2
7234E	08/22/87	Th Ox,TiO2 Std.BEL; FES coated/baked/sintered in new facility. G7225 first sol-gel made in new facility on new apparatus.	11-5	G7225, (0/50/50,+10), 9	8cts @ rpm		2@400	30@650inO2	Fat2
7236A	08/24/87	Th Ox,TiO2 Std.BEL w/500Å Ti cap; FES coat/bake/sinter in new facility. G7225 first sol-gel made in new facility on new apparatus.	14-1	G7225, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	Fat2
7236B	08/24/87	Th Ox,TiO2 Std.BEL w/500Å Ti cap; FES coat/bake/sinter in new facility. G7225 first sol-gel made in new facility on new apparatus.	14-2	G7225, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	Fat2

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7236C	08/24/87	Th Ox,TiO2	15-1	G7225, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	Fat2
	Std.BEL w/500Å Ti cap; FES coat/bake/sinter in new facility. G7225 first sol-gel made in new facility on new apparatus.								
7236D	08/24/87	Th Ox,TiO2	15-2	G7225, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	Fat2
	Std.BEL w/500Å Ti cap; FES coat/bake/sinter in new facility. G7225 first sol-gel made in new facility on new apparatus.								
7239A	08/27/87	Th Ox,TiO2	74-1	G7194, (0/50/50,+10), 45	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at UNM, 2 LPM O2. .								
7239B	08/27/87	Th Ox,TiO2	74-1	G7194, (0/50/50,+10), 45	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked at UNM; Sintered at Krysalis, 5 LPM O2. .								
7239C	08/27/87	Th Ox,TiO2	74-1	G7225, (0/50/50,+10), 14	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at UNM, 2 LPM O2. .								
7239D	08/27/87	Th Ox,TiO2	74-1	G7225, (0/50/50,+10), 14	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked at UNM; Sintered at Krysalis, 5 LPM O2. .								
7239E	08/27/87	Th Ox,TiO2	90-1	G7194, (0/50/50,+10), 45	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked at Krysalis; Sintered at UNM, 2 LPM O2. .								
7239F	08/27/87	Th Ox,TiO2	90-1	G7194, (0/50/50,+10), 45	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at Krysalis, 5 LPM O2. .								
7239G	08/27/87	Th Ox,TiO2	90-1	G7225, (0/50/50,+10), 14	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked at Krysalis; Sintered at UNM, 2 LPM O2. .								
7239H	08/27/87	Th Ox,TiO2	90-1	G7225, (0/50/50,+10), 14	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at Krysalis, 5 LPM O2. .								
7239I	08/27/87	Th Ox,TiO2	90-2	G7194, (0/50/50,+10), 45	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at UNM, 2 LPM O2. .								
7239J	08/27/87	Th Ox,TiO2	90-2	G7194, (0/50/50,+10), 45	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked at UNM. .								
7239K	08/27/87	Th Ox,TiO2	90-2	G7225, (0/50/50,+10), 14	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at UNM, 2 LPM O2. .								
7239L	08/27/87	Th Ox,TiO2	90-2	G7225, (0/50/50,+10), 14	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked at UNM. .								
7240A	08/28/87	Th Ox,TiO2	90-3	G7225, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at Krysalis, 5 LPM O2. .								
7243A	08/31/87	Th Ox,TiO2	90-3	G7243, (0/50/50,+10), <1	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at Krysalis, 5 LPM O2;80°F,35%RH. .								
7244A	09/01/87	Th Ox,TiO2	90-3	G7243, (0/50/50,+10), 1	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at Krysalis, 5 LPM O2;74-78°F. .								
7244B	09/01/87	Th Ox,TiO2	90-4	G7243, (0/50/50,+10), 1	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at Krysalis, 5 LPM O2;81°F,65%RH?. .								
7245A	09/02/87	Th Ox,TiO2	90-4	G7243, (0/50/50,+10), 2	8cts @ rpm		2@400	30@650inO2	?
	Coated/Baked/Sintered at Krysalis, 5 LPM O2;65°F,68%RH. .								
7247A	09/04/87	Th Ox,TiO2	18-1	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH. .								
7247B	09/04/87	Th Ox,TiO2	18-2	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH. .								
7247C	09/04/87	Th Ox,TiO2	18-3	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH. .								
7247D	09/04/87	Th Ox,TiO2	18-4	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH. .								

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7247E	09/04/87	Th Ox,TiO2	18-5	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH. .								
7247F	09/04/87	Th Ox,TiO2	16-1	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;500Å Ti cap over BEL. Anna's 1st FES coats - cts 2 thru 5.								
7247G	09/04/87	Th Ox,TiO2	16-2	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;500Å Ti cap over BEL. Anna's 1st FES coats - cts 2 thru 5.								
7247H	09/04/87	Th Ox,TiO2	16-3	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;500Å Ti cap over BEL. Anna's 1st FES coats - cts 2 thru 5.								
7247I	09/04/87	Th Ox,TiO2	16-4	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;500Å Ti cap over BEL. Anna's 1st FES coats - cts 2 thru 5.								
7247J	09/04/87	Th Ox,TiO2	16-5	G7243, (0/50/50,+10), 4	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;500Å Ti cap over BEL. Anna's 1st FES coats - cts 2 thru 5.								
7248A	09/05/87	Th Ox,TiO2	17-1	G7243, (0/50/50,+10), 5	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;400Å Ti cap over BEL. .								
7248B	09/05/87	Th Ox,TiO2	17-2	G7243, (0/50/50,+10), 5	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;400Å Ti cap over BEL. .								
7248C	09/05/87	Th Ox,TiO2	17-3	G7243, (0/50/50,+10), 5	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;400Å Ti cap over BEL. .								
7248D	09/05/87	Th Ox,TiO2	17-4	G7243, (0/50/50,+10), 5	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;400Å Ti cap over BEL. .								
7248E	09/05/87	Th Ox,TiO2	17-5	G7243, (0/50/50,+10), 5	8cts @ rpm		2@400	30@650inO2	Fat2
	Coated in chem lab;____°C,____%RH;400Å Ti cap over BEL. .								
7251A	09/08/87	06M061-1	?	G7243, (0/50/50,+10), 8	8cts @ rpm		2@400	30@650inO2	512
	Coated in chem lab;77°F,42%RH;500Å Ti cap over BEL. .								
7251B	09/08/87	06M061-2	?	G7243, (0/50/50,+10), 8	8cts @ rpm		2@400	30@650inO2	512
	Coated in chem lab;77°F,42%RH;500Å Ti cap over BEL. .								
7251C	09/08/87	06M061-7	?	G7243, (0/50/50,+10), 8	8cts @ rpm		2@400	30@650inO2	512
	Coated in chem lab;77°F,42%RH;500Å Ti cap over BEL. .								
7251D	09/08/87	06M061-11	?	G7243, (0/50/50,+10), 8	8cts @ rpm		2@400	30@650inO2	512
	Coated in chem lab;77°F,42%RH;500Å Ti cap over BEL. .								
7253A	09/10/87	Nitride#11	NONE	G7243, (0/50/50,+10), 10	8cts @ rpm		2@400	NA	NA
	Wafers for National Semiconductor. .								
7253B	09/10/87	Oxide#23	NONE	G7243, (0/50/50,+10), 10	8cts @ rpm		2@400	NA	NA
	Wafers for National Semiconductor. .								
7253C	09/10/87	Nitride#2	YES	G7243, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	NA
	Wafers for National Semiconductor. .								
7253D	09/10/87	Oxide#13	YES	G7243, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	NA
	Wafers for National Semiconductor. .								
7253E	09/10/87	06M061-13	?	G7243, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	512
	500Å Ti cap over BEL. .								
7253F	09/10/87	06M061-14	?	G7243, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	512
	500Å Ti cap over BEL. .								
7253G	09/10/87	06M061-17	?	G7243, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	512
	500Å Ti cap over BEL. .								
7253H	09/10/87	06M061-20	?	G7243, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	512
	500Å Ti cap over BEL. .								

FILM ID	DATE COATED	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL TYPE
7253I	09/10/87	06M061-21	?	G7243, (0/50/50,+10), 10	8cts @ rpm		2@400	30@650inO2	512
	Std BEL. .								
7254A	09/11/87	Nitride	NONE	G7243, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	NA
	Wafers for National Semiconductor;no solvent pre-wash. .								
7254B	09/11/87	Oxide	NONE	G7243, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	NA
	Wafers for National Semiconductor;no solvent pre-wash. .								
7254C	09/11/87	Th Ox,TiO2	CB8295	G7243, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	Fat2
	. .								
7254D	09/11/87	Th Ox,TiO2	CB8296	G7243, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	Fat2
	. .								
7254E	09/11/87	Th Ox,TiO2	CB8297	G7243, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	Fat2
	. .								
7254F	09/11/87	Th Ox,TiO2	CB8298	G7243, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	Fat2
	. .								
7254G	09/11/87	Th Ox,TiO2	CB8299	G7243, (0/50/50,+10), 11	8cts @ rpm		2@400	30@650inO2	Fat2
	. .								
7258A	09/15/87	Th Ox,TiO2	F002-6	G7243, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	Ti/Pt/Ti 850/1200/250Å cold/cold/cold. .								
7258B	09/15/87	Th Ox,TiO2	F002-10	G7243, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	Ti/Pt/Ti 850/1200/250Å cold/hot/cold. .								
7258C	09/15/87	Th Ox,TiO2	F002-13	G7243, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	Ti/Pt/Ti 850/1200/250Å hot/hot/cold. .								
7258D	09/15/87	Th Ox,TiO2	F002-16	G7243, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	Ti/Pt/Ti 850/1200/250Å hot/cold/cold. .								
7258E	09/15/87	Th Ox,TiO2	F002-2	G7243, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	Ti/Pt/Ti 850/1200/250Å cold/cold/cold. .								
7258F	09/15/87	Th Ox,TiO2	F002-8	G7243, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	Ti/Pt/Ti 850/1200/250Å cold/hot/cold. .								
7258G	09/15/87	Th Ox,TiO2	F002-11	G7243, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	Ti/Pt/Ti 850/1200/250Å hot/hot/cold. .								
7258H	09/15/87	Th Ox,TiO2	F002-15	G7243, (0/50/50,+10), 15	8cts @ rpm		2@400	30@650inO2	Fat2
	Ti/Pt/Ti 850/1200/250Å hot/cold/cold. .								
7265A	09/22/87	Th Ox,TiO2	_____	G7259, (0/50/50,+10), 6	5cts @ 2000rpm		2@400	30@650inO2	NA
	Coating thickness trials:bake_____µm,sint_____µm. .								
7265B	09/22/87	Th Ox,TiO2	_____	GI7264A, (0/50/50,+10), 1	5cts @ 2000rpm		2@400	30@650inO2	NA
	Coating thickness trials:bake_____µm,sint_____µm. .								
7265C	09/22/87	Th Ox,TiO2	_____	G7264, (0/50/50,+10), 1	5cts @ 2000rpm		2@400	30@650inO2	NA
	Coating thickness trials:bake_____µm,sint_____µm. .								
7268A	09/25/87	Th Ox,TiO2	_____	GI7264A, (0/50/50,+10), 4	5cts @ 3000rpm		2@400	30@650inO2	Fat2
	Thickness/etch rate study;post bake_____Å,post sint_____Å. .								
7268B	09/25/87	Th Ox,TiO2	_____	G7264, (0/50/50,+10), 4	5cts @ 4000rpm		2@400	30@650inO2	Fat2
	Thickness/etch rate study;post bake_____Å,post sint_____Å. .								
7272A	09/29/87	Th Ox,TiO2	_____	G7259, (0/50/50,+10), 13	8cts @ 2000rpm		2@400	30@650inO2	Fat2
	Illinois gel study - Control. .								
7272B	09/29/87	Th Ox,TiO2	_____	G7264, (0/50/50,+10), 8	4cts @ 3000rpm		2@400	30@650inO2	Fat2
	Illinois gel study - Krysalis 0.5M gel. .								

FILM ID	DATE COATED	SUBSTRATE DESCRIPTION	BEL TYPE	SOL-GEL ID, (Composition), & AGE in days	COATS & SPIN SPEED	t°C/%RH @ Spin	BAKE PROFILE	SINTER PROFILE	TEL TYPE
7272C	09/29/87	Th Ox,TiO2	_____	GI7264B, (0/50/50,+10), 8,1	5cts @ 4000rpm		2@400	30@650inO2	Fat2
	Illinois gel study - 4mol/mol hydrolyzed,basic. .								

Exhibit B

KRYSALIS CORPORATION Krysalis Confidential

FAILURE ANALYSIS REPORT

SUBJECT: SEM and Optical Microscopic study of selected low failure rate die on Wafer#7148A
DATE: June 16, 1987
BY: Leo Chapin

Following is preliminary data on failure analysis of wafer#7148A. Dave Eaton provided us with a bit failure map of 6 selected die having relatively low, random (but repeatable) bit failures. Two of six die were examined and photographed using the Hitachi 450 SEM at UNM. All six die were examined using the Nikon Optiphot in differential interference contrast (Nomarski) mode at X1000 magnification.

DIE#	FAILED BIT	DESCRIPTION OF FAILURE
0,+7	44,7	Missing TEL on bottom cell
	57,6	Blister on bottom cell
0,+4	4,7*	TEL filament bridge with 5,7
SEM	5,7*	(see above)
photos	17,1*	Blister on cell
	23,1*	Small blisters on cell
	48,5*	Blister (adjacent cell,49,5, also blistered)
	56,6*	? (adjacent good cell,57,6, blistered)
+2,+1	8,1*	? nothing apparent
SEM	56,4*	Missing FES in capacitors
photos	56,5*	" " " "
	57,4*	" " " "
	57,5*	" " " " NOTE: Some adjacent cells which tested good also had FES missing from capacitors.*
	63,7*	Blister
+5,+3	51,0	Small blister on top cell
	53,7	Blister on bottom cell
	60,0	Blister on top cell
+5,+2	25,1	Blister on top cell
	31,1	Very small blisters(5) on top cell
	32,2	? (blister on 33,2)
	48,7	Blister on bottom cell
	49,7	Medium blisters(2) on bottom cell
	51,1	Blister on bottom cell
	52,7	Blister on bottom cell
	63,3	Blister on bottom cell; 6+small to v.small blisters on top cell

-2,-1	36,1	V.small blister (large blister on 37,2)
	49,0*	Blister on cell
	50,6*	? nothing apparent
	54,5*	Blister on cell
	55,4*	Blister on cell
	56,7*	? nothing apparent

The blisters on failed bits, except where noted, had a diameter that was typically 2/3 to 3/4 the width of BEL. On die# +2,+1 a fast (and somewhat subjective) survey was made of blister size. The blisters were catagorized as + (larger than), = (same size), and - (smaller than) relative to the typical failed bit blister. Of the 1024 capacitors viewed, one had a blister in the + (larger than) catagory, 21 had blisters in the = (same size) catagory, and 209 had blisters in the - (smaller than) catagory (this last catagory is the most subjective since cells with few very small blisters were not counted).

The asterisk following the FAILED BIT address indicates that SEM and/or optical microscope photos were made. In addition to these photos the following were made:

+2,+1	9,2	Good bit with large (= same as) blister but partly off BEL
	8,2b	Metal over TEL for comparison with 8,1 (? nothing apparent but bad)
	22,5t	"Good bit" with missing TEl over top cell
-2,-1	-,-	Typical area
=2,-3	-,-	Typical area

All photos related to failure analysis are kept in a binder (titled "Failure Analysis Reports") with a copy of the report.

Efforts are underway to catagorize blister size (and other defects) more objectively.

Some 7148A film data:

FES COATING LOG Krysalis Confidential

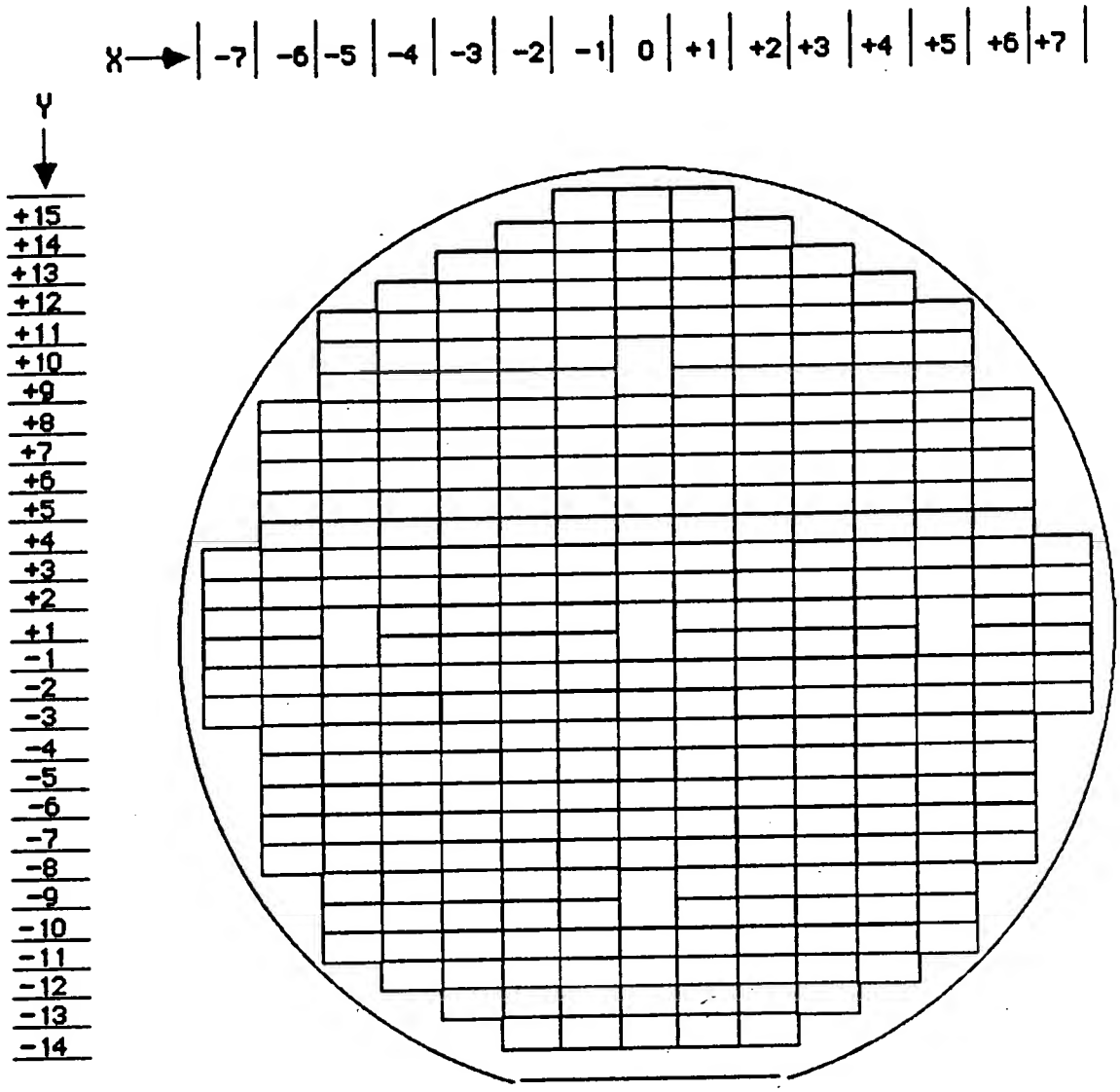
FILM ID	SUBSTRATE	BEL	TEL	BAKE	ANNEAL	DAY MADE
7148A	...ECD512A	..B86	..512	..2@400	..30@650in02	05/28/87

G7110(8/40/60,+10);8cts;38 days old
NOTES:CMOS ECD512A with 8/40/60,+10

Attached is the wafer die addressing scheme used in this report (comments solicited and accepted, perhaps).

16JUN87:LNC

ECD512A Die Address Guide (X,Y)



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